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Hybrid Printing Process for Fabricating Flexible
Polysilicon TFTs

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Hybrid Printing Process for Fabricating Flexible Polysilicon TFTs

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Chapter 1

Introduction

1. Background and motivation

1.1. Recent development and demand of the internet of things (IoT)

As the integrated circuit has become increasingly powerful, the concept that embedded intelligence could penetrate everything around us has become increasingly realistic. Since it was first conceptualized in 1988 at Xerox PARC, ubiquitous computing is now a reality. When these devices can communicate with one another, the market for the Internet of Things (IoT) will become another reality. Some markets for the IoT are beyond our imagination in size and scope, such as wearables. Image sensors in clothing that can detect ambient viruses that send an alarm to your cell phone. To realize this capability, instead of a complex, rigid device, something far simpler is required, which is flexible but robust, perhaps single-purpose and disposable, including sensors that capture information and wireless communication that sends it.

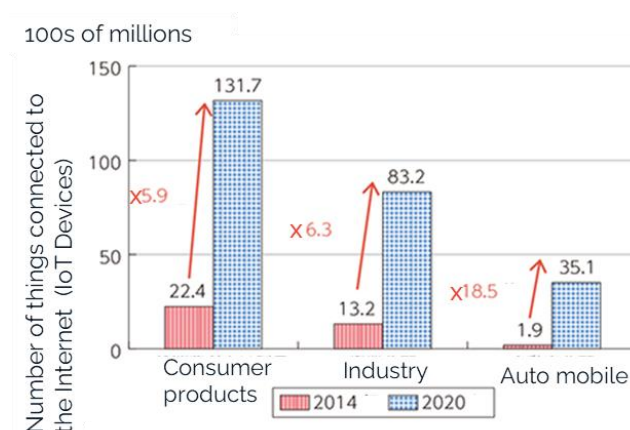


Figure 1.1 Number of things connected to the internet

(<https://www.soumu.go.jp/johotsusintokei/whitepaper/ja/h27/html/nc254110.html>)

Because of the demand for billions and trillions of limited-function devices, new methods of mega-volume production must be discovered. Similarly, to address environmental concerns, per unit material and energy consumption must be vastly reduced. Academe and industry alike have realized that one solution to this need is through printed electronics. In printed electronics, far fewer transistors can be created per area, even in -limited function devices. Furthermore, printing could be achieved based on standard industry methods at far lower material and energy costs than traditional semiconductors, and they could be printed on a flexible substrate, which is the goal of the research that I present in this thesis.

1.2. Conventional semiconductor process vs. printing process

To achieve thin, flexible, and robust devices with limited logic wireless capability, poly silicon thin film transistors (TFT) and the use of stainless-steel foil as a substrate were researched. To achieve mega volumes with a low step count and low per-unit material and energy consumption, different print methodologies and roll-to-roll manufacturing were researched. For low-power wireless communication, -near field communication (NFC) was chosen.

Figure 1.2 below compares conventional versus printed integrated circuit (IC) development. The conventional methodology is based on a subtractive process. A metal or insulator layer is first laid over the substrate using vacuum equipment. The insulator is then coated with a photoresist, exposed through a mask, and then developed. The metal layer was then etched, and the resist layer was removed. This printing methodology is an additive process. The functional layer is patterned by printing, and the precursor inks are sintered. Compared with the conventional process, this printing process requires a much lower step count and much lower material and energy consumption. It also does not require high capital cost lithography, vacuum, or ion implantation equipment.

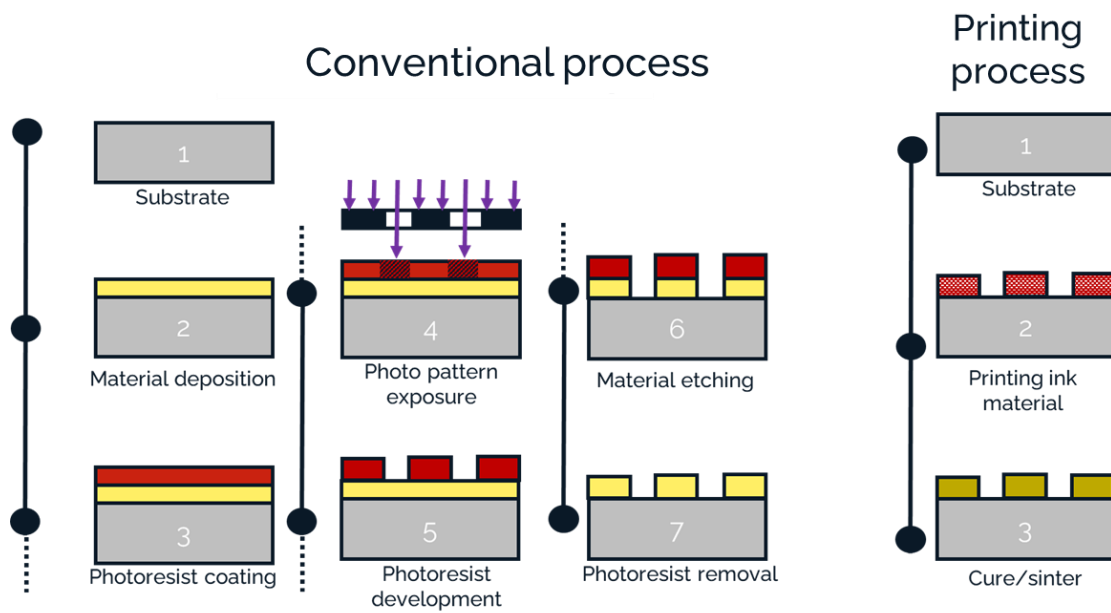


Figure 1.2: (a) Conventional semiconductor process, (b) printing process

In the electronics industry, printing has traditionally been used to print solder paste and etching resist for printed circuit boards (PCB). In the last few decades, there has been an increasing amount of research on printing as an additive process used to fabricate active and passive devices in the electronics industry. Today, printing is used to develop electrical and optical inks that are deposited on substrates and to fabricate active or passive devices, such as TFTs, capacitors, and resistors. There is on-going research using these low-cost printed devices to develop flexible displays, wearable sensors, and the IoT. Printed electronics have also been developed in combination with flexible electronics because both are compatible with the roll-to-roll process, which is another driver of very low-cost devices. Typically, conventional semiconductors justify their much higher costs by providing greatly increased performance. Table 1.1 shows variety of printing and coating technique and their characteristics.

Table 1.1 Various printing and coating techniques and their classifications [2]

	Printing				Coating		
Classification	Contact				Non-contact		
Method	Gravure	Offset	Flexo	Screen	Inkjet	Slot-die	Spin
Throughput (m ² /s)	3-60	3-30	3-30	2-3	0.01-0.5	2-3	5
Resolution (Lines/cm)	20-400	100-200	60	50	60-250	NA	NA
Ink viscosity [cps]	50-200	50-200	50-200	500-50k	1-20	1-50k	1-100
Material waste	Low	Low	Low	Low	Low	Low	high

1.3. Flexible substrate

As a substrate, stainless steel foil has been researched because of its flexibility, resiliency, and ability to withstand high operating temperatures, which are required by sintering in the printing process. Figure 1.3 (a) and (b) compare silicon wafers with stainless steel foils as substrates. On the one hand, the production of silicon wafers emits a great deal of carbon dioxide. On the other hand, stainless steel foil emits far less carbon dioxide, mainly because a large part of it is recycled. In addition, to be thin, silicon wafers need to go through an expensive back grinding process that makes them brittle. Stainless steel foil, however, can be produced to be as thin as 10 μm .

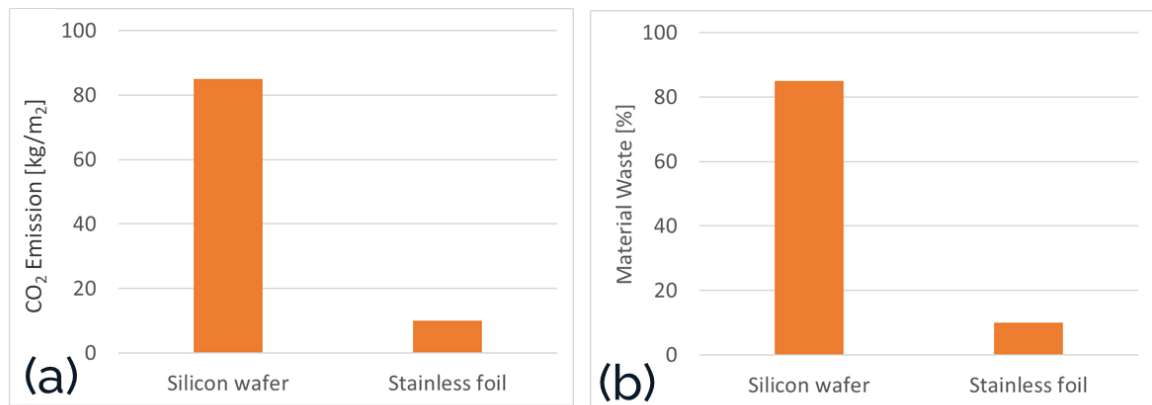


Figure 1.3 (a) CO₂ emission of production of silicon wafer and stainless-steel foil, (b) material waste of silicon wafer and stainless foil substrate for packaging

In addition, due to its flexibility and durability, stainless steel foil can be extended beyond sheet manufacturing to roll-to-roll manufacturing. Finally, as demonstrated in Figure 1.4, in impact tests, ICs fabricated on stainless steel foil were more robust than those fabricated on silicon substrates.

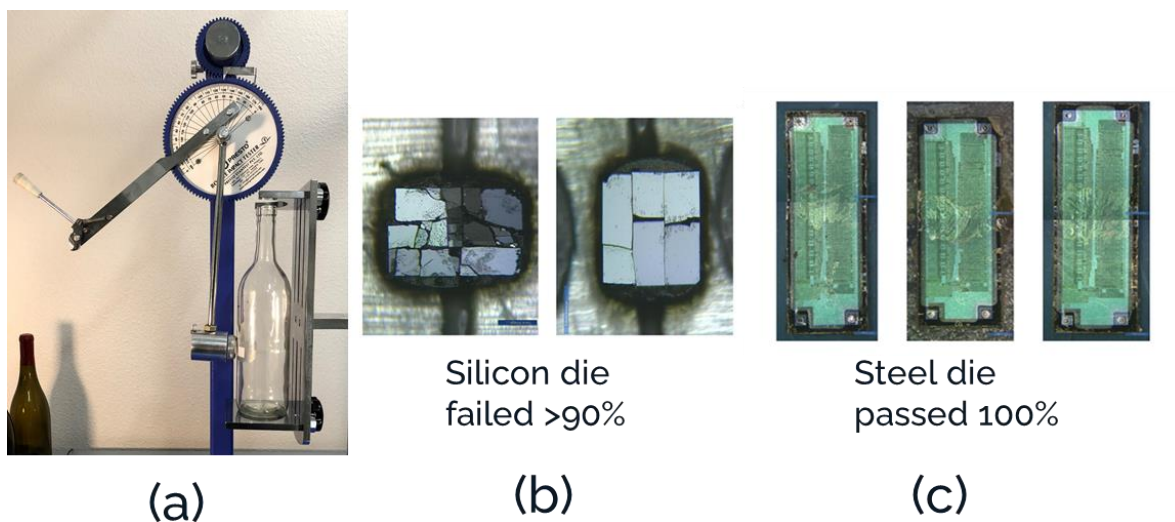


Figure 1.4 (a) Photographs of bottle impact test, (b) silicon dies after impact test, and (c) steel die after impact test

1.4 Printable semiconductor materials

1.4.1. *Organic semiconductors*

Organic semiconductor materials, such as pentacene and polyacetylene, can be easily prepared as liquid solutions for printable inks. To fabricate electric circuits, these materials can be treated at low temperatures to be electronically active, which allows the use of inexpensive but durable plastic films as flexible or stretchable substrates. Flexible organic devices have been created for various applications, such as robot skins ^[3], flexible biosensors ^[4], electronic banknotes ^[5], and flexible displays ^[6], among others. However, organic materials have multiple disadvantages ^[7] compared with inorganic semiconductor materials. First, the charge carrier mobilities of organic semiconductors are generally $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This is insufficient for more demanding and complex circuitry, such as logic circuits in communications or sensor detection. Second, due to their chemical nature, organic semiconductor materials exhibit poor chemical stability when exposed to water, oxygen, and light. Therefore, the devices degrade quickly over time.

1.4.2. *Metal oxide semiconductor*

Metal oxide precursors, alkoxide, and organic salts are also easily dissolved in organic solvents to be used as solutions at room temperature, and they can be deposited on flexible substrates for similar applications. These materials can achieve typical mobilities in an order of magnitude that is higher than organic semiconductors, at approximately $10\sim 30\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ^[8-11]. However, materials such as ZnO have multiple disadvantages. They do not offer the fast recombination of photogenerated electron-hole pairs, and they are only active with UV light. Finally, they are prone to photo corrosion.

1.4.3. *Silicon ink*

Silicon is the most established and stable semiconductor material. Not only does its high performance compare with organic and metal oxide semiconductor materials, but it has also been used in many infrastructures. Moreover, because of its long history, there is a great deal of knowledge about silicon. Analytical methods, circuit designs, and chemicals all support the fabrication of silicon devices. In bringing new technology or materials to industry, the use of established infrastructures is an efficient and successful strategy.

there are two options for a precursor of silicon: silicon nanoparticles or a hydrosilane compound in the liquid phase. In the early 1970s, Hengge et al. studied cyclic silane compounds and concluded that cyclopentasilane (CPS) was a precursor of amorphous silicon^[12]. This research was rediscovered in the early 2000s. In our research, both paths were considered, synthesized to formulate inks, and then tested. With respect to silicon nanoparticle ink, it was exceedingly difficult to remove the surfactant that modified the nanoparticles so that they could dissolve into organic solvents, which made its use attractive. CPS, however, proved to be more promising.

In the same period, in 2006, Shimoda et al. demonstrated that TFTs could be fabricated using CPS and its polymer as silicon precursors^[13]. Since then, this research has expanded. Ishihara et al. demonstrated that single-grain crystal TFTs could be fabricated using a grain filter technique and excimer laser crystallization^[14-17]. These TFTs demonstrated high electron mobility as high as $600 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. However, this process required trench holes in the silicon wafer and was therefore not suitable for low-cost devices. Subsequently, Trifunovic et al. fabricated polysilicon TFTs using CPS ink on a paper substrate^[18,19]. In this case, direct laser patterning and crystallization were performed on a CPS-coated paper substrate. Unfortunately, the mobility of the TFTs produced was too low for logic circuits. If a large-area laser system could be integrated with a glovebox, this technique could have the potential for use in low-cost disposable devices. Finally, to reduce the consumption and

cost of CPS ink and to improve its printing resolution, Masuda et al. demonstrated the nanoimprinting of CPS and other fabrication techniques, such as nanoimprinting or direct electron beam writing ^[20-21]. Table 1.2 shows variety of semiconductor material and their characteristics.

Table 1.2: Comparison of solution-based transistor technologies

	Organic [7]	Metal-oxide [8-11]	Poly-Si [14-17]	Si wafer [18]
Electron Mobility($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	0.01	10	200-600	1500
Temperature ($^{\circ}\text{C}$)	<100	<100	>350	>1000
Stability	O ₂ , H ₂ O	Light	Stable	Stable
Substrate	PET	Polyimide	Any	Itself
Performance	Poor	Fair	Moderate	High
Other				Back grind Fragile

2. Research objectives

Based on past research, the overall objective of this study, which extended over several years, was to discover a polysilicon TFT fabrication method that provided performance that was high enough for logic circuits with low energy consumption and high-volume printing on flexible substrates, which are requirements in the consumables market. Table 1.3 shows a summary of the development phase of this study. In this dissertation, Chapter 2 presents the laboratory phase, and Chapters 3–5 present the pilot study. Chapter 6 presents some considerations for future roll-to-roll production.

Table 1.3: Summary of the development phase of this study

Stage	Laboratory scale (This study)	Pilot scale (This study)	Mega scale (Future)
Purpose	Silicon ink development Less step count Proof of concept	Realistic process Less step count R2R expandable Middle-size volume production Commercial product	Further scale up Eliminate clean room
Substrate	Wafer	Sheet	Roll to roll
Process	All print	Print/litho hybrid	Print/litho hybrid
New development	Silicon and other inks Top gate fabrication scheme	Stainless steel foil substrate Slot-die coating silicon ink Screen-printed dopant	R2R equipment Low-cost ink
Volume	NA	10s Millions die/yr	Billions die/yr

2.1. Ink development and inkjet printing for polysilicon TFTs

The research objective of this first effort was to establish a fabrication process for high-performance TFT devices entirely by printing, thus eliminating the need for conventionally expensive vacuum deposition, ion implantation, and lithography. To realize this objective, the focus was on using the potential of end-to-end inkjet printing as a proof-of-concept that required the development of silicon ink using high-purity CPS and other electrically functional novel electronic inks, including dopant ink, palladium silicide ink, and silver ink.

2.2. Study of the hybrid process

In the second effort, the research objective was to apply the results of the print-only research above to establish an alternative low step-count process that was compatible with roll-to-roll manufacturing for billions and trillions of units at scale. The initial target product of this research was an NFC logic circuit, which required radio-frequency (RF, 13.56 MHz) capable circuits and materials, high mobility, and low power circuits with adequate transistor density. For this purpose, self-aligned top-gate complementary metal oxide semiconductor (CMOS) and laser crystalized polysilicon thin film transistors (TFT) were adopted to fabricate the logic circuits. Our process goals were therefore to discover the lowest step count and lowest material and energy consumption method possible while maximizing printing over traditional semiconductor processing while providing excellent overlay capability. The print-only effort using end-to-end inkjet printing proved inadequate for achieving the 4- μm design rules. Therefore, complementary metal oxide semiconductor (CMOS) TFT fabrication using a hybrid lithography/printing process flow was proposed. To build a hybrid process, the following three key materials and processes were investigated.

- To achieve a thin, unbreakable form factor with low cost and excellent dimensional stability, stainless-steel foil was chosen as a substrate. Critical dimension control, flatness, surface quality, process durability, and high-temperature barrier layers were examined.

- To achieve high throughput and high mobility silicon film formation of the active layer, the slot-die coating of silicon ink was investigated. CPS-based ink coating versus plasma-enhanced chemical vapor deposition (PECVD) was compared, and the dihydrogen bake condition for crystallization using a solid-state laser was investigated.
- To eliminate the ion implant process, which is high maintenance, energy consumption, and not roll-to-roll compatible, a novel formulation of semiconductor grade screen printable dopant N⁺ and P⁺ inks and their process were studied. Printability, a doping process with a high temperature anneal, and controlling counter doping were evaluated.

2.3. Considering further scale and polytetrasilane ink

- For further scale to mega volume, expanding the sheet line to the roll-to-roll line was planned. The risk of bending and fabricating sensitive devices on stainless steel through roll-to-roll lines was evaluated.
- To remove the bottle neck in supply silicon ink, the application of polytetrasilane ink synthesized in-house using proprietary polymerization to fabricate polysilicon film was evaluated.

3. Outline

The outline of this dissertation is shown in Figure 1.4.

Chapter 2 presents the study of silicon inks, N⁺ and P⁺ dopant inks, palladium inks, and silver nanoparticle inks. Then, the fabrication process of the first fully inkjet printed N⁺ and P⁺ polysilicon TFT structure is established.

Content of chapter 2

- Ito, M. and Kamath, A. Fabrication and Characterization of Entirely Inkjet-Printed Polysilicon Thin Film Transistors. *Flex. Print. Electron.* (2020)

Chapter 3 presents the study of flexible, low-cost, lightweight, mechanically strong stainless steel foil in a 300 mm² substrate that can be used in high-temperature processes above 800 °C. The mass production of NFC logic circuits consisting of low-cost CMOS polysilicon TFT was achieved by adopting an impurity diffusion process using screen printing requiring high-temperature annealing. The articles describes the possibility of expanding to roll-to-roll manufacturing.

Content of chapter 3

- Ito, M. and Kamath, A., Large Area, High Temperature Stainless Steel Foil Substrate for Manufacturing Low-cost CMOS Polysilicon TFTs, *J. Soc. Inf. Disp.*, 1-10 (2022)

Chapter 4 presents a study of a large area of 300 mm² polysilicon film formation using slot die coating of silicon ink and crystallized by a solid laser.

Content of chapter 4

- Ito, M. and Kamath, A., Slot-die Coating of Silicon Ink for Manufacturing Logic Circuits, *Jpn. J. Appl. Phys.* 60, 101001 (2021).

Chapter 5 presents a study of screen-printable N⁺ and P⁺ dopant inks to improve performance and manufacturability. This study evaluated the characterization of inks, printability, and doping performance, which were optimized for TFT fabrication.

Content of chapter 5

- Ito, M. and Kamath, A., Formulation and characterization of screen printable dopant ink, *Flex. Print. Electron.* (2021)
- Chandra, A., Takashima, M., Montague, M., Li, J. and Kamath, A., *MRS Advances*, 1(14), 965–970 (2016).

Chapter 6 presents the consideration of further scaling using the roll-to-roll process and polytetrasilane ink

Content of chapter 6

- Chandra, A., Takashima, M., Li, J., Beck, P., Bruner, S., Tinsley, D., Kamath, A. (2017). Considerations and Methodology to Determine R2R Manufacturing and Scaling of Electronic Devices on Flexible Stainless Steel Foil Substrates. *MRS Advances*, 2(18), 1029–1036. doi:10.1557/adv.2017.274
- Ito, M. and Kamath, A., Polysilicon TFTs fabricated using poly-tetrasilane ink., *MRS Commun.*, doi.org/10.1557/s43579-022-00152-1 (2022)

Chapter 7 presents the process flow of TFTs in integrating stainless steel substrate, slot-die coating silicon ink, screen printing dopant, and conventional film formation patterning process. As a result, the world's first high-performance printed TFT volume production was realized and applied in industrial use. This process was novel and industrially valuable. The significance of establishing a material and manufacturing method that produced process-saving, high-performance TFTs on a flexible, robust substrate that greatly reduced the amount of energy consumption, chemical solution, and ink required was a significant contribution to industry.

Appendix: Characterization of CMOS polysilicon TFTs, NFC logic circuits, and their products.

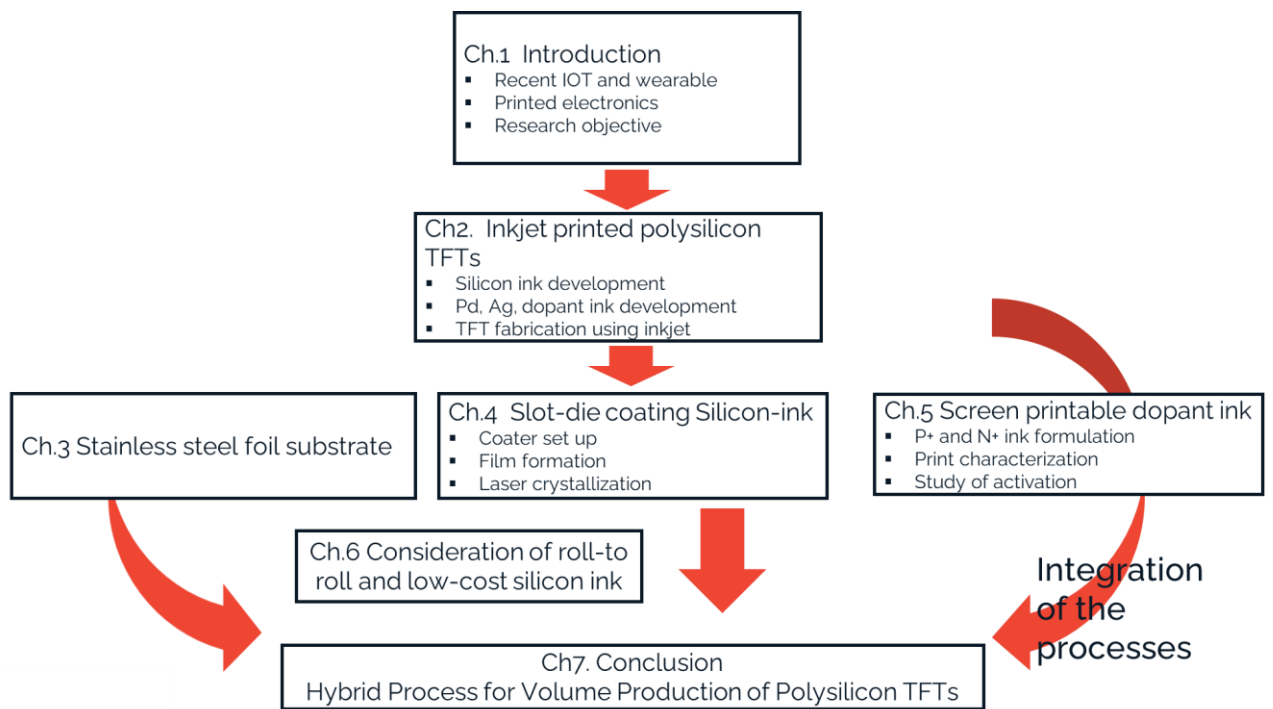


Figure 1.4: Outline of the dissertation

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Chapter 2

Study of High Purity Ink for Entirely Inkjet-Printed TFTs

1. Introduction

1.1. Research objective

The research objective of the first step was to develop materials and fabrication schemes for polysilicon TFT devices entirely by printing, thus eliminating the need for conventionally expensive vacuum deposition, ion implantation, and lithography. To achieve this objective, the focus was on using the potential of end-to-end inkjet printing to develop a proof-of-concept production line that required the development of silicon ink using high purity CPS-based ink and other electrically functional novel electronic inks, including dopant ink, palladium silicide ink, and silver ink.

1.2 Ink jet printing

To fabricate TFTs, inkjet printing was chosen as the primary printing technique. Inkjet printing is a common printing technology used in most home office printers. One of the main advantages of inkjet printing by prototyping additive electronics devices is that it is digital. Hence, whenever a design change occurs, the new design can be printed on the spot without additional tooling, which reduces iteration time. Digital inkjets rely on ejecting tiny droplets from hundreds of tiny nozzles on a print head in quick succession to form a pattern on a substrate. The piezo inkjet uses piezo elements to send a shock wave through the ink to eject a droplet. Figure 2.1 shows a cross-section image of the typical piezo electric inkjet head. Piezo elements are a type of ceramic that deforms when exposed to a voltage potential. Piezo inkjet printers use this property by sending voltage waveforms that have been tuned

specifically to the geometry of the fluid path, the ink being ejected, and the size of the droplets, which typically range from 10pl to 30pl.

Because it requires only 1 ml of ink to start printing. In the early stage of developing inks, we could synthesize only a few grams of ink, so it was desirable to use a printing technique that required less volume. Additionally, a small desktop printer (Dimatix, Fig. 2.2(a) (b)) was easily integrated into a glove box (Mbraun, Fig. 2.2(b)) when a special ambient was required to avoid ink degradation.

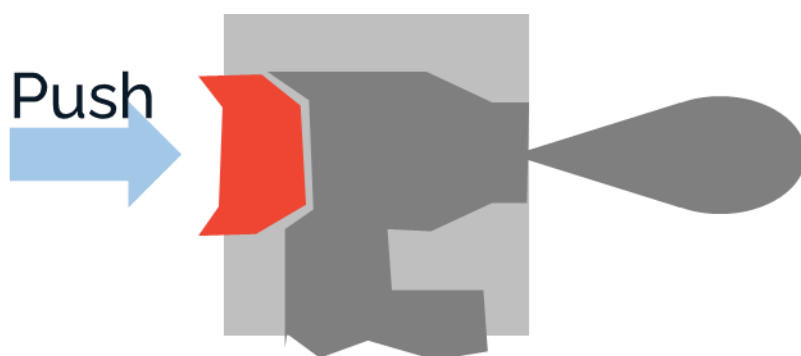


Figure 2.1: Cross-section image of piezo-type inkjet printhead

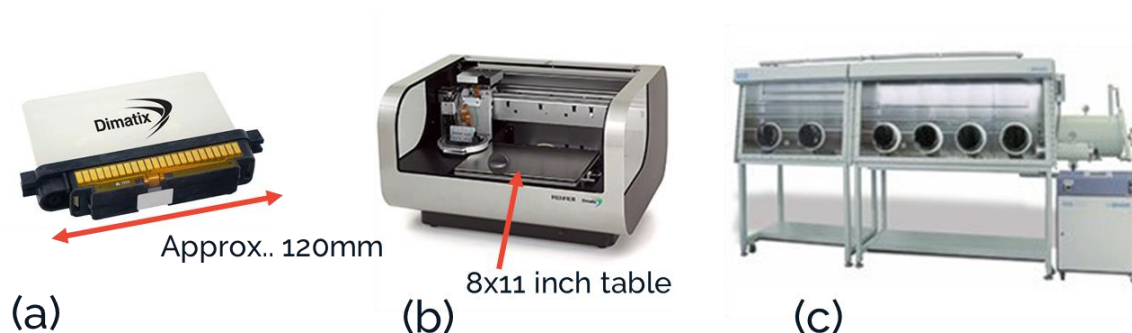


Figure 2.2: (a) Inkjet head, (b) tabletop inkjet printer (Dimatix), and (c) glovebox (Mbraun) to keep silicon ink and dopant ink in nitrogen gas

1.3 Characterization scheme of ink for ink jet

Inks used in print electronics are formulated using precursors of functional layers, such as semiconductors, insulators, and metals. Appropriate solvents and surfactants are added if needed. In drying the ink solution, if the evaporation of the solvent is not even on the surface, temperature, and surface tension (ST) are decreased in localized areas. This phenomenon causes the convection and migration of the liquid film, which is called the Marangoni flow, and eventually forms an uneven film thickness. Figure 2.3 shows the Marangoni flow ^[1].

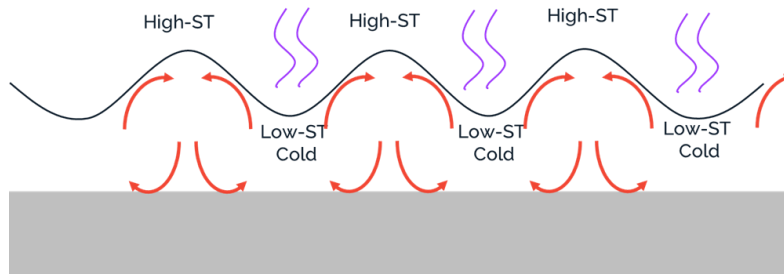


Figure 2.3: Model of Marangoni flow during the evaporation of solvent from a coated wet film

The Marangoni number (Mg) is a dimensionless number that compares the rate of transport due to Marangoni flow with the rate of transport of diffusion ^[2]:

$$Mg = \frac{\Delta\sigma}{\Delta T} * \frac{1}{\eta\alpha} * L * \Delta T$$

where

σ : surface tension [N/m]

L : characteristic length [m]

α : thermal diffusivity [m²/s]

η : dynamic viscosity [kg/(s·m)]

ΔT : temperature difference [K]

This issue is common in the coating industry, and multiple ways are applied to suppress the flow. The selection of the solvent and surfactant is a vital factor in suppressing Marangoni flow.

Multiple inks were evaluated and screened for compatibility, firing, and pattern formation characteristics. Figure 2.3 shows the screening flow of ink in an inkjet. First, the compatibility of the precursor with the solvents was evaluated by observing clearness or precipitation. Second, 5 μl of ink were drop casted on a substrate such as silicon wafer, and its spread and film quality were observed. Ink that spread widely or formed a hazy film was not accepted. Third, the inks were loaded into the inkjet heads, and ink firing was observed using a camera that was integrated with the inkjet head. Ink that did not run long enough without misdirection or nozzle clogging was not accepted. Finally, the inks were printed, and the printed patterns were compared with the original artwork. Inks that spread widely or were beaded up were not accepted. The ink that passed all evaluations was used to print the TFT structures in this study.

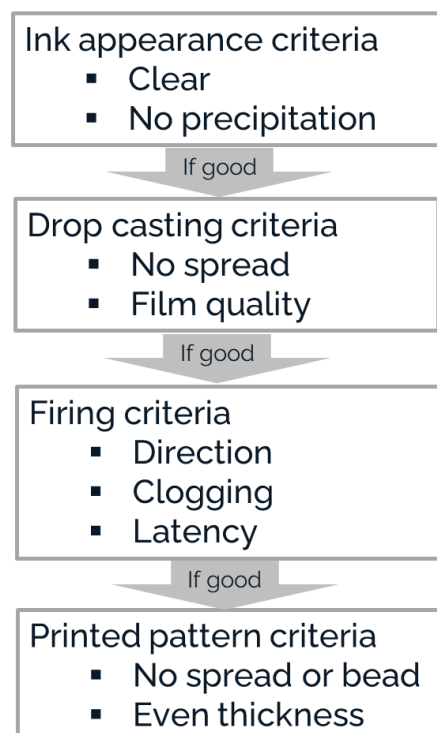


Figure 2.3: Inkjet ink screening flow

1.4 Chemistry of ink precursors

Figure 2.4(a) shows the synthesis path of CPS presented by Hengge. Using diphenyl-dichlorosilane as the starting material, CPS was synthesized in three steps. Amorphous silicon forms from CPS after polymerization and heat treatment above 350 °C [3]. Shimoda et al. used UV irradiation to polymerize CPS, as shown in Fig. 2.2(b), to formulate silicon ink [4]. In this study, a modified Hengge's synthesis and purification process of monomer CPS in-house was used as the precursor of silicon. A proprietary heterogeneous catalyst was developed to polymerize CPS, as shown in Fig. 2.4(c), for better control of polymerization and to modulate the viscosity of the silicon ink for inkjet printing [5].

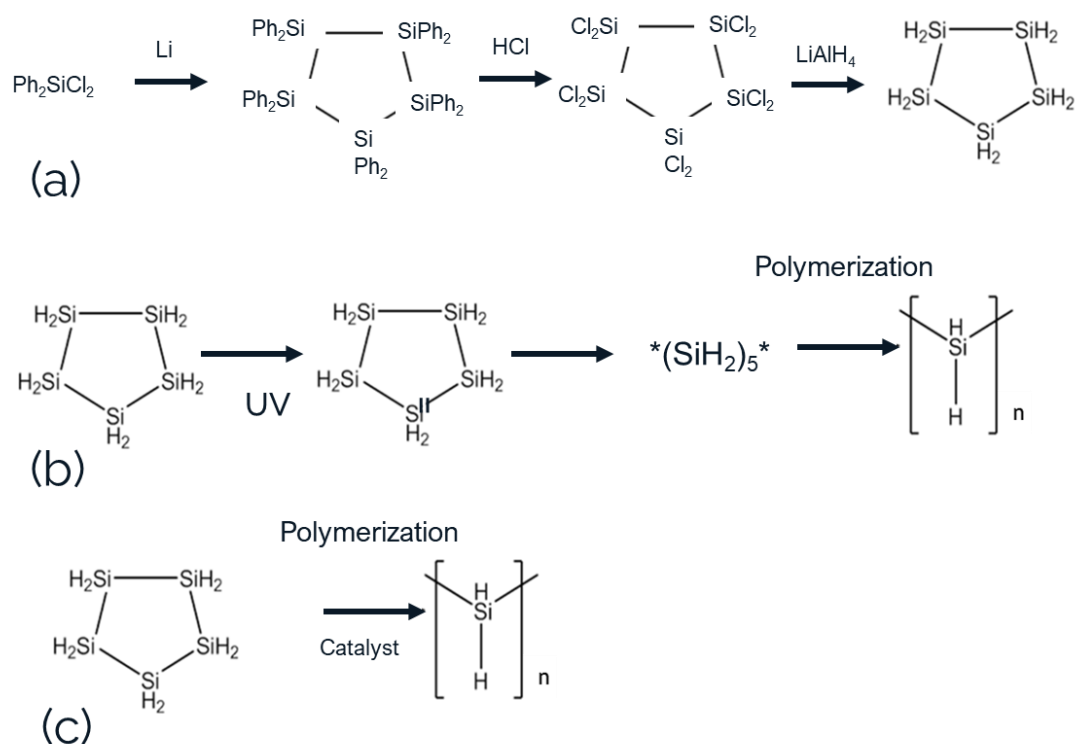


Figure 2.4: (a) Synthesis path of cyclopentasilane, (b) UV polymerization of CPS, and (c) CPS polymerization using a catalyst

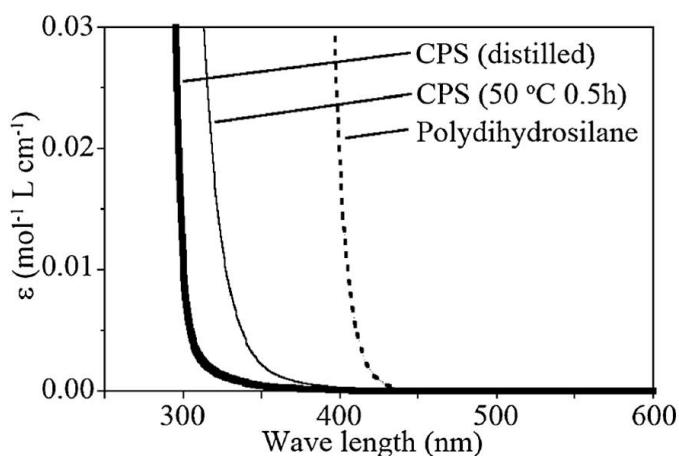


Figure 2.5: Absorption spectra of freshly synthesized CPS, CPS under accelerated aging at 50 °C for 30 min, and polydihydrosilane ^[5]

Poly-CPS at an approximate molecular weight ($M_n = 1,000$) is a liquid form that can be dissolved in solvents and flows due to the thermal-induced Marangoni effect during the heating process. For this reason, the wet film of poly-CPS needs to be irradiated with UV to increase its molecular weight and viscosity to stabilize it before thermal curing. Therefore, the solvent required to formulating the ink needs to be transparent and inert in UV irradiation. Cyclohexane was used to synthesize CPS because it is known to be inert to CPS. Additionally, the UV absorption of cycloalkanes, including cyclohexane and cyclooctane, is known to be the lowest in any organic solvent, and it is not absorbed above 200 nm. It does not have a double bond that absorbs UV and generates radicals or an oxygen constituent, as peroxides and oxygen radicals can react with silane. Figure 2.6 shows the Fourier-transform infrared spectroscopy (FT-IR) spectrum of CPS in terpinene-4-ol ink after UV irradiation and a hard bake for comparison with CPS in cyclooctane. The hard-baked film formed from the CPS ink in terpinene-4-ol showed peaks of CH, O_xSiH, and SiOSi and revealed contamination by the solvent. Therefore, in this study, it was important to choose solvents that were compatible with CPS and did not contaminate the film formed during UV irradiation and the hard bake.

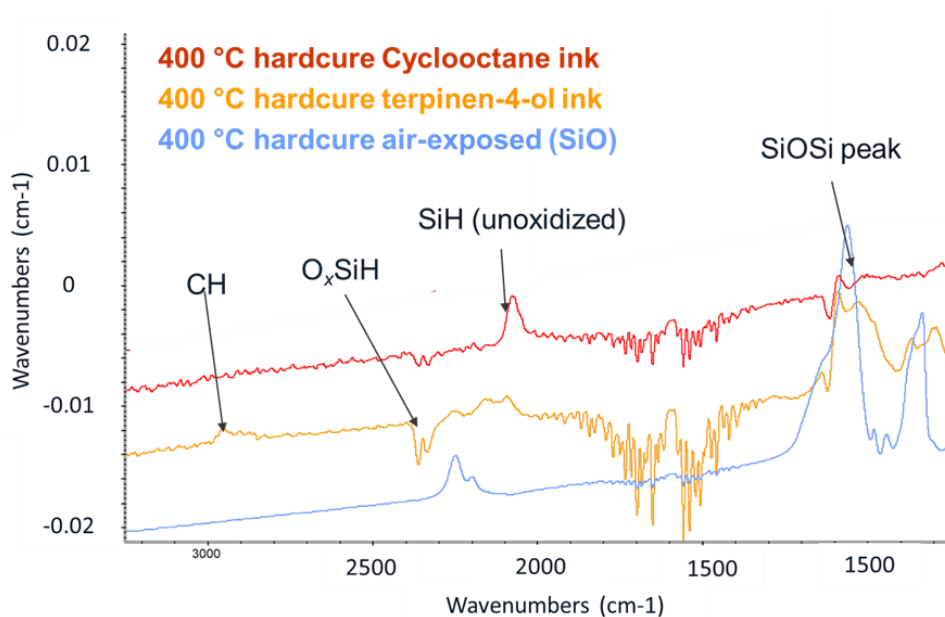


Figure 2.6: FT-IR spectrum of CPS ink in cyclooctane and terpinene-4-ol after hard bake

The boiling point was another factor to consider in choosing an adequate solvent for the application technique. Cyclooctane has a boiling point of 150 °C, which is typical of solvents used for spin coating. Because cis-decalin has a high boiling point of 190 °C, it was chosen to formulate the inkjet ink to avoid drying and clogging the inkjet nozzles. The solvents were purified to remove oxidizing compounds that could potentially contaminate the silicon film and otherwise reduce carrier mobility.

To evaluate ink purity and optimize process parameters, amorphous silicon films formed by spin coating were first studied. A spin coating recipe with simultaneous UV irradiation was developed to form films directly from poly-CPS. A low-pressure mercury grid lamp and exhaust were integrated with a spin-coater. The analytical results of spun films were conveyed to the chemistry team to improve synthesis, purification procedure, and handling to avoid contamination during storage and spin coating.

Pyrolysis at various annealing temperatures of spun poly-CPS film was studied by Masuda [6]. Figure 2.7 shows the pyrolysis investigated using thermal gravimetry (TG) and differential gravimetry (DTG). The DTG measurements showed major weight losses at 100, 200, and 300 °C [5]. Weight loss at 100 °C represents the evaporation of solvent, at 200 °C represents monomer CPS, and at 300 °C represents hydrogen produced by decomposition. Figure 2.8 shows the transformation process from poly-CPS to amorphous silicon during the process step.

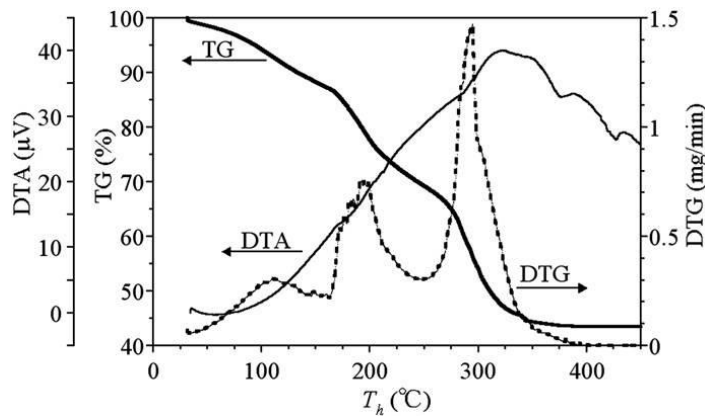


Figure 2.7: TG, DTA, and DTG measurement results of the analysis of various thermal annealing temperatures of liquid silicon [5]

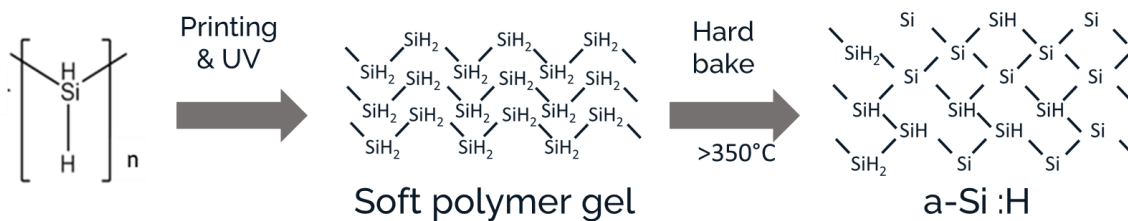


Figure 2.8: Transformation process from poly-CPS to amorphous silicon

In this study, an XeCl-based (308 nm) laser was used to crystalize the silicon. All resulting protuberances had to be managed or eliminated; otherwise, they could lead to gate oxide coverage and reliability issues in active silicon.

Boron and phosphorous dopant inks were developed for N⁺ and P⁺ doping. Spin-on dopants ^[7] (Honeywell Inc.) were used as the base materials for formulating the dopant inks. P-8545 was used to formulate the N⁺ ink with phosphorous, and B-30 was used to formulate the P⁺ ink with boron. The primary solvent for these materials was ethanol, which is not suitable for ink jetting, as it quickly evaporates and tends to clog inkjet nozzles. Moreover, ethanol's lower surface tension and higher volatility created a self-induced Marangoni effect ^[8], which caused the ink to rush out of the region where the droplets fell onto the oxide surface. To formulate the ink used in inkjet printing in well-defined areas, ethanol was replaced by a low volatility solvent, and a silicone polymer surfactant was added to suppress the Marangoni flow ^[9]. Boron oxide in the printed P⁺ ink was hygroscopic and reacted with moisture in the air at room temperature to form boric acid (boiling point = 300 °C). Due to the volatile nature of boric acid at the diffusion temperature, the duration of boron oxide exposure to ambient air had to be controlled; otherwise, it would reduce the ability of the printed boron dopant to activate silicon ^[10]. To ensure a reproducible P⁺-doped silicon, all moisture trapping phenomena had to be avoided. Printing and soft curing of the P⁺ ink needed to be operated in a nitrogen or dry air environment, and the duration of exposure to ambient air before thermal annealing had to be minimized.

Because the contact between the silver and doped polysilicon was relatively poor ^[11], an ink was required to form a silicide as an ohmic contact between the silver interconnect and the doped polysilicon. Metals such as nickel, cobalt, titanium, tungsten, and palladium can form silicide ^[12]. In this experiment, palladium was chosen because it can diffuse through native oxide (SiO₂) in a reducing ambient environment, which eliminated the need for a pre-sputter etch for ohmic contact formation ^[13, 14]. Therefore, a process of forming palladium silicide

(Pd₂Si) was developed. Because palladium chloride is reduced to palladium metal by annealing in a forming gas (N₂/5%H₂), palladium chloride ink was formulated as a precursor of palladium metal, which was then used to form palladium silicide with doped polysilicon.

Silver NP ink was developed to form an interconnecting layer. It is known that the fine particularization of metals reduced to nanometer size reveals properties that differ from bulk materials, which is due to the comparatively significant increase in the proportion of atoms with large surface energy exposed to nano-sized particle surface area. Various features, such as the improvement in catalytic activity and the effect of the melting point, became evident. The property that the melting point is lowered has been examined for a long time. The expression of Pawlow^[15,16] models the relationship between size and melting point. Figure 2.9 shows the formula predicting that the melting point will decrease rapidly from 10 nm.

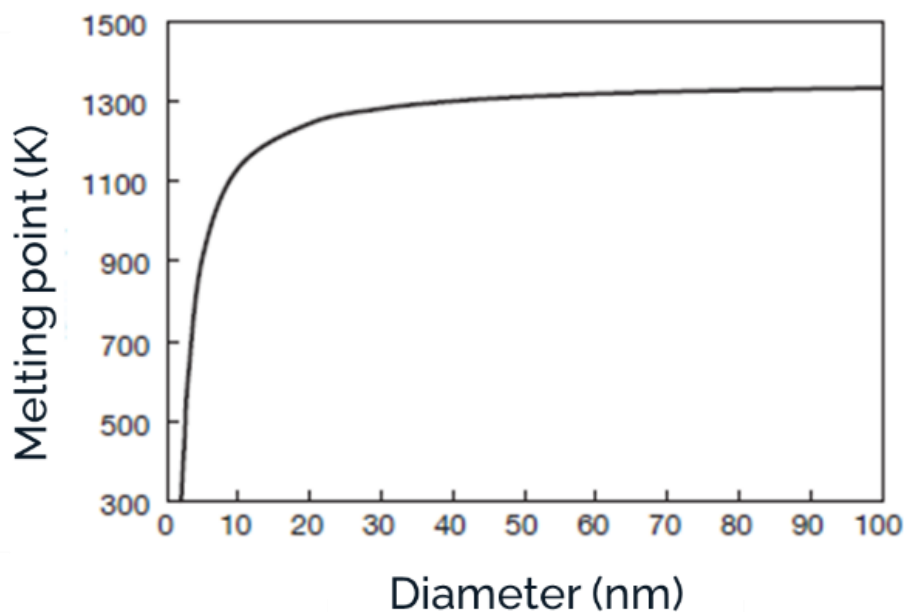


Figure 2.9: Melting point of silver particles versus diameter

In the early 2000s, Oda et al. demonstrated the synthesis of silver NP by trapping metal vapor in solvent and lowering temperature ^[17]. Since then, there has been an increase in research on sintering materials for bonding electronic components and creating fine wiring at low temperatures. Multiple techniques are applied to make silver NP, the first of which is milling. The milling technique is the simplest and least expensive method. However, in this technique, it is difficult to make even-diameter nanoparticles from bulk materials. The second method involves trapping metal vapor in an organic solvent. In this method, it is easy to make low impurity particles of nano size. However, the size distribution tends to be wide, and the required equipment tends to be large and costly. The third method is liquid phase synthesis. In this method, metal ions in a solvent are reduced using a strong reducing agent. This can be a low-cost method to produce nanoparticles. In this study, silver nanoparticles were synthesized by reducing silver oxide dissolved in a solvent and surfactant in-house.

2. Experiments

2.1. Ink preparation

2.1.1. *Silicon ink*

CPS was synthesized using a modified Hengges' scheme ^[3], which was then purified and polymerized to semiconductor-grade levels. The resulting polymer was analyzed using gel permeation chromatography (GPC), a capillary viscosity meter, and inductively coupled plasma mass spectrometry (ICPMS) to measure the molecular weight, viscosity, and trace metal content. The cyclooctane (> 99%, Sigma-Aldrich) or cis-decalin (> 99%, Sigma-Aldrich) were washed using sulfuric acid and then distilled over sodium to remove remaining traces of water. A 15-vol% poly-CPS solution in cyclooctane was prepared for spin coating. This was dispensed using a glass syringe through a 0.2 μm PTFE disk filter on an SiO_2 coated silicon wafer. After a short spreading rotation at 500 revolutions per minute (rpm), high-speed rotation at 1,000 rpm, UV irradiation, and exhaust were simultaneously enabled. The coated silicon film was baked in a muffle oven under a nitrogen gas flow via a gas purifier at 400 °C for 20 min to reduce the hydrogen. The incorporated impurity levels were determined using ICPMS analysis and secondary ion mass spectroscopy (SIMS) of the spin-coated film. All operations were performed in a glove box that maintained oxygen and moisture levels below 5 ppm. Next, a 15 vol% poly-CPS solution in cis-decalin was prepared for inkjet printing, and the ink was dispensed into the cartridge of an inkjet head through a 0.2 μm polytetrafluoroethylene (PTFE) disk filter.

2.1.2. *Dopant ink*

To formulate the N⁺ ink, P-8545 was first poured into a flask with a rotary evaporator. Then an equal weight of diethylene glycol monobutylether (> 98%, Sigma-Aldrich) was added. As the ethanol in the P-8545 evaporated, it was replaced by diethylene glycol monobutylether. Then 0.00 2wt% of polydimethylsiloxane surfactant (Botanisil S-18, D-D

Chemco) was added to suppress the Marangoni effect. The B-30 was processed in a similar manner to formulate the P+ ink.

2.1.3. *Palladium chloride ink*

Palladium chloride ink was formulated using 2 wt% palladium chloride (Sigma Aldrich) dissolved in deionized water/diethyl glycol butyl ether (99%, Sigma Aldrich, 15/85). Then, using a vortex mixer, the solution was mixed in a vial for 10 min, allowed to settle for 12 h, and then filtered prior to loading it into the inkjet cartridge. Commercially available palladium precursors (Palladium film, Emulsitone Company) and palladium chloride ink formulated with diethyl glycol butyl ether were tested for comparison purposes.

2.1.4. *Silver ink*

Silver NPs were synthesized from silver oxide using liquid- phase reactions. Silver oxide (99%, Sigma Aldrich) was reduced using 1-Decene (95%, Sigma Aldrich), 2-ethylhexanoic acid (99%, Sigma Aldrich), and the proprietary fatty acid surfactant in the solvent, which formed silver NPs covered with the surfactant. The reaction mixture was then centrifuged with isopropyl alcohol (IPA). The decan supernatant was subsequently mixed with hexane and IPA and centrifuged again. The nanoparticle diameters were determined using transmission electron microscopy (TEM). To formulate the ink, 20 wt% of the silver NPs were dissolved in cis-decalin and dispensed into a cartridge through a 0.2 μm PTFE disk filter.

2.2. TFT fabrication

A top-gate self-aligned process flow using a polysilicon gate and printed dopants was developed. A diagram of the fabrication flow is illustrated in Fig. 2.10. Silicon wafers 100 mm in diameter were cleaned and thermally oxidized, which resulted in a 1 μm SiO_2 film as the field oxide. Both surface cleaning and preparation were performed before the printing process. Before printing the active island, the oxide surface was first treated with

hexamethyldisilazane (HMDS) and then exposed to UV/ozone with a low-pressure mercury lamp as the surface modification. The contact angle of the cis-decalin was measured using a drop-shaped analyzer after the modification process.

The 15 vol% poly-CPS silicon ink prepared in cis-decalin was printed using an inkjet printer (Dimatix, 10 pL nozzle) with ink pattern dimensions of 60 μm x 1200 μm in a glove box in a nitrogen gas environment. Printed poly-CPS patterns were irradiated simultaneously by UV (50 mJ/cm^2 at 365 nm) from a spot UV curing system was integrated with the inkjet printer. The printed wafer was immediately hard baked at 420 $^{\circ}\text{C}$ for 20 min, and a further dehydrogenation bake was performed at 550 $^{\circ}\text{C}$ for 15 h in ambient nitrogen. Parallel and perpendicular cross-sectional profiles were measured using a profilometer (Tencor).

Because it was stable in air, the wafer with active silicon islands was removed from the glove box after the hard-baking process. The surface of the active island was oxidized (750 $^{\circ}\text{C}$ for 0.5 h, O_2) and then dipped in diluted hydrofluoric acid (HF 50:1, 60 s) to preclean it before it was crystallized using XeCl excimer laser irradiation (1200 mJ/cm^2). The wafer was then loaded in a tube furnace and annealed at 850 $^{\circ}\text{C}$ in N_2/O_2 to form a 35 nm gate oxide. The silicon gate layer was then printed with silicon ink and baked in the identical process used for the active channel layer.

The gate oxides on the source and drain were removed using a 50:1 HF bath for 7 min. Then a 200 μm diameter N^+ ink was printed on top of the cross point of the island and the gate, as shown in Fig. 2.10 (top view). This was soft-cured at 100 $^{\circ}\text{C}$ for 10 min. The printing and soft-cure operations were performed in the glove box in ambient nitrogen. The wafer was then rapidly thermally annealed (RTA) at 850 $^{\circ}\text{C}$ for 5 min in ambient nitrogen.

After precleaning the wafer using HF (500:1), the palladium chloride ink was printed outside the printed dopant area and then soft cured at 230 $^{\circ}\text{C}$ for 2 min, followed by annealing at 650 $^{\circ}\text{C}$ for 2 h in the forming gas (5% hydrogen gas in argon gas, Plaxair). After annealing

with the forming gas, X-ray diffraction (XRD) on the spun palladium chloride ink with various solvents on the spun poly-CPS film was used to determine the formation of the palladium metal and Pd_2Si .

Silver NP ink was printed on the silicide area to form an interconnection pattern before being thermally cured on a hotplate at 300 °C for 10 min. Sheet resistivity was measured using four-point probes on appropriate test structures.

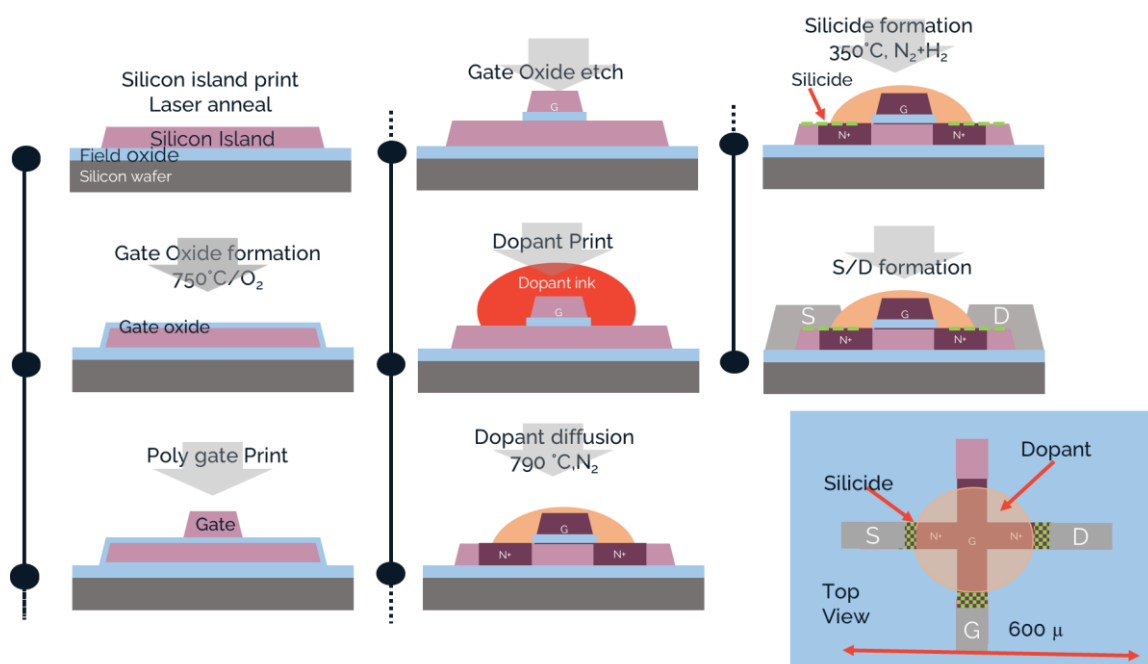


Figure 2.10: Diagram of the fabrication of TFTs using inkjet printing

3. Results and discussion

3.1. Characterization of inks and fabricated films

Figure 2.11 shows the GPC spectrum of CPS and poly-CPS. After polymerization, peaks of dimers and trimers were observed. The molecular weight of poly-CPS was $M_w = 910$ g/mol, and its viscosity was 6–8 mPa, while that of the inkjet ink was 2–3 mPa·s at 20 °C. The shelf life of the formulated ink exceeded several months with no change in appearance and viscosity when it was stored below -20 °C. Inks prepared with other solvents, such as alcohol, ether, ketone, and ester, demonstrated turbidity immediately or a day after formulation and were not used. Table 2.1 shows the trace metal impurity of poly-CPS measured with ICPMS. A typical hard-cured film was analyzed using SIMS and was shown to contain minimal quantities of carbon, oxygen, and other impurities, as shown in Table 2.2. The learning from and optimization of the spin-coating process were directly applied to the ink jet formulation.

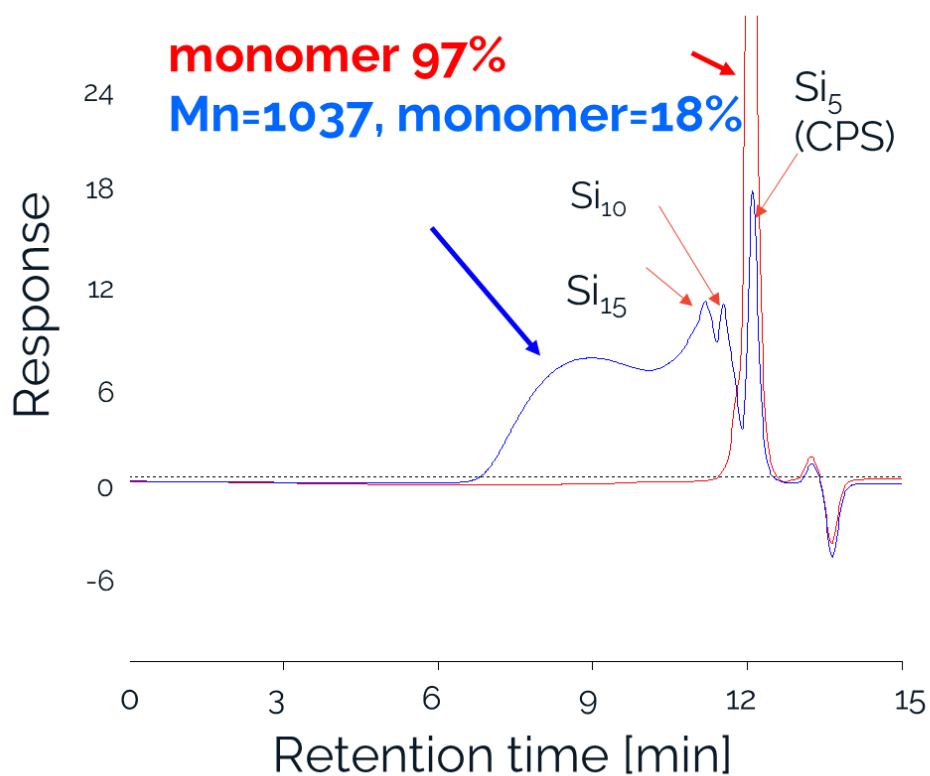


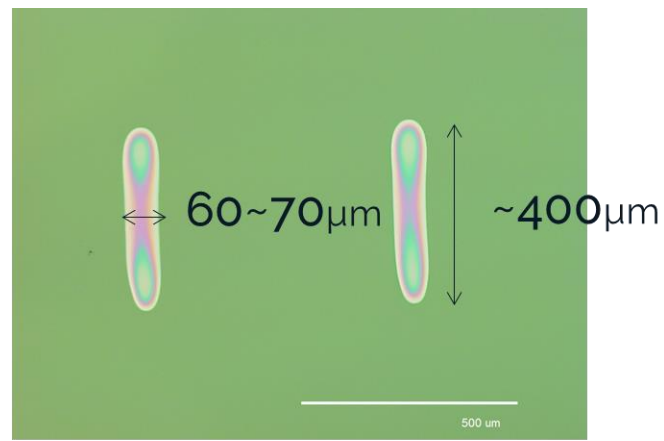
Figure 2.11: GPC spectrum of CPS and poly-CPS

Table 2.1: Trace metal impurity of poly-CPS measured with ICPMS

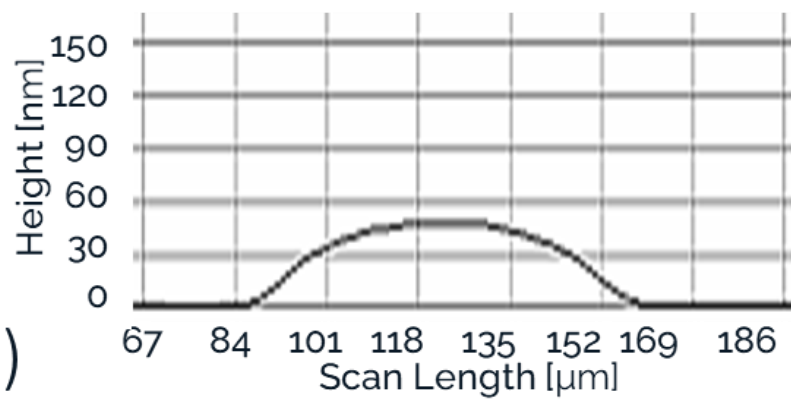
Atom	Al	Ca	Mg	K	Na	Cr	Cu
Concentration [PPB]	83	<0.5	<20	<20	78	19	9.5

Table 2.2: Concentration of the negative and positive species in a hard-cured poly-CPS ink measured using SIMS

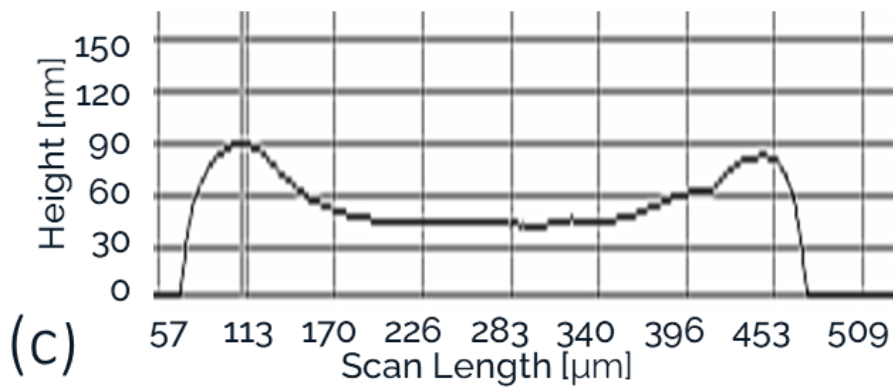
Atom	C	O	N	Cl	P	Na	Mg	Al	Cr	Cu
Concentration [PPM]	4000	1000	70.10	64.50	0.88	0.02	0.02	0.04	0.02	0.04



(a)



(b)



(c)

Figure 2.12: (a) Optical microscope top-view image of the printed island, (b) cross-sectional profile of the cured island measured using a Tencor profilometer, and (c) profile along the length of the cured island

Figure 2.12(a) shows a microscope image of the inkjet-printed active islands, which formed a dog bone shape. Parallel and perpendicular cross-sectional profiles are shown in Figure 2.12(b) and (c). The thickness at the center of the peak was 45–65 nm.

The dogbone-shaped printed film was thicker in the area surrounded by the pinned edge, suggesting a coffee-ring effect. Figure 2.13(a) shows the coffee ring, which resembled a spilled drop of coffee dried on a solid surface. It left a dense ring-like stain along the perimeter. This was caused by the capillary flow induced by the pinned edges during the evaporation process ^[18]. Figure 2.13(b) shows the mechanism of outward flow during evaporation. Figure 2.13(b)(I) shows the result of evaporation liquid without solid content. The edge of the droplet retracted as evaporation proceeded. Fig. 2.13(b)(II) shows the pinned contact line caused by the drying of the solution with a solid content. The compensating flow went into a thinning liquid film. As a result, the center of the spilled droplet became thinner in case (II), and the edge of the droplet received more solution, which left a thicker film near the perimeter edge.

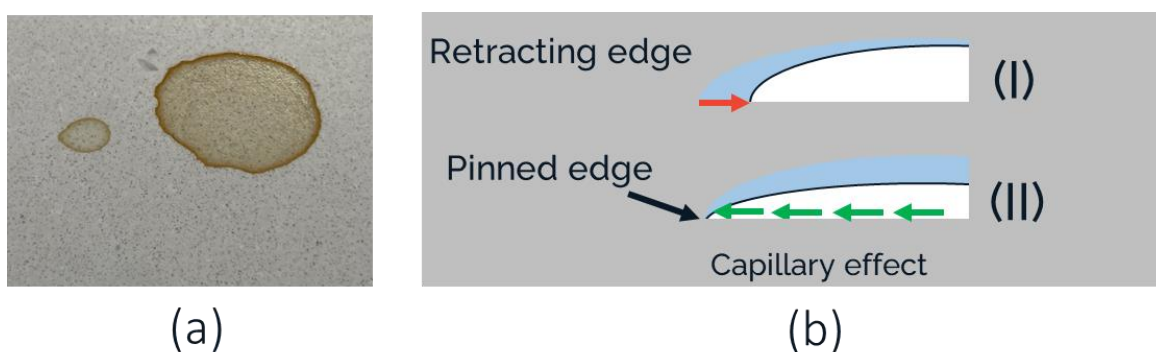


Figure 2.13: (a) Coffee stain after drying refers to the coffee ring, (b) mechanism of outward flow during evaporation

Using spin-coated films, laser crystallization was studied as the first step in achieving high mobility. Figure 2.14(a) shows a cross-section of the formation of bubbles in the film. Irradiation from the excimer laser can lead to this formulation, due to hydrogen in the film. However, the dehydrogenation bake ^[19] at 550 °C for 15 hours in a nitrogen flow prevented the films from forming bubbles, as shown in Fig. 2.14(b). Table 2.3 shows that the hydrogen content decreased to less than 1 atm% after the dehydrogenation bake, which was low enough that the dehydrogenated film did not show any bubbles after the excimer laser irradiation. The same hard-cure and dehydrogenation bake conditions were applied to the inkjet-printed poly-CPS layer. This also decreased the hydrogen content to less than 1 atm%. Table 2.3 shows the results of the SIMS analysis comparing hydrogen content before and after the dehydrogenation anneal. Figure 2.14(c) shows a cross-section transmission electron microscopy (TEM) image of the crystallized active island. No bubbles were observed, but a crystalline lattice was observed.

Table 2.3: SIMS analysis of the silicon film for the post-dehydrogenation bake

Deposition method	Hard bake	Dehydrogenation bake	C [atm%]	H [atm%]	O [atm%]	N [ppm]
Spin coat	420 °C	NA	0.03	8.0	0.02	1
Spin coat	20 min in N ₂ gas	550 °C 15 hr in N ₂ gas	0.01	0.5	0.02	7
Inkjet	420 °C	NA	0.04	4.4	0.38	2
Inkjet	20 min in N ₂ gas	550 °C 15 hr in N ₂ gas	0.01	0.82	0.02	3

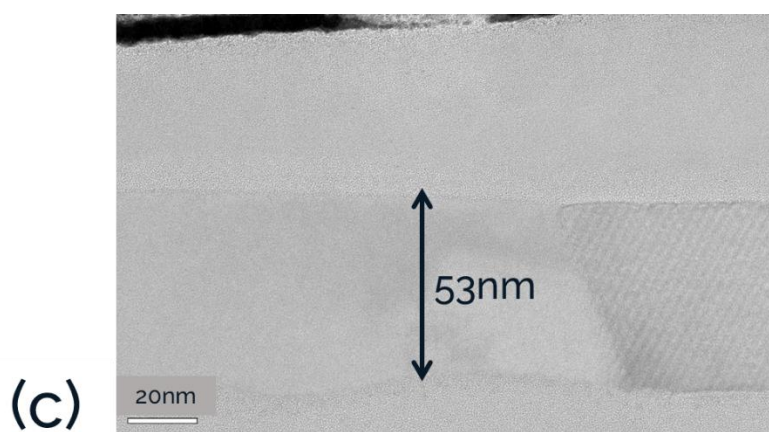
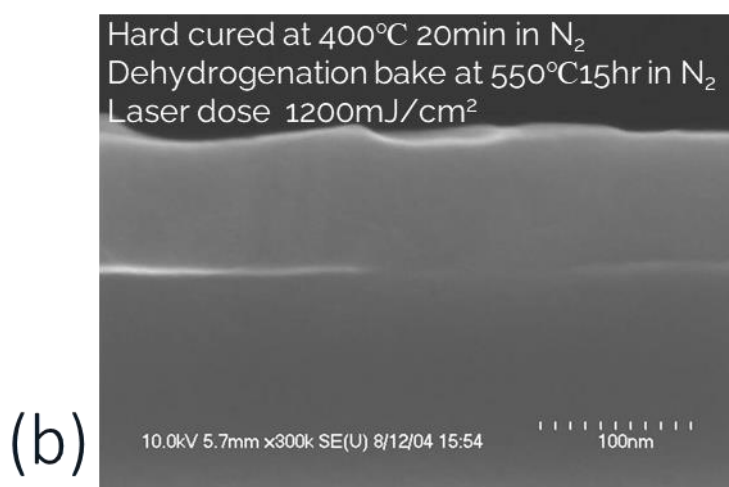
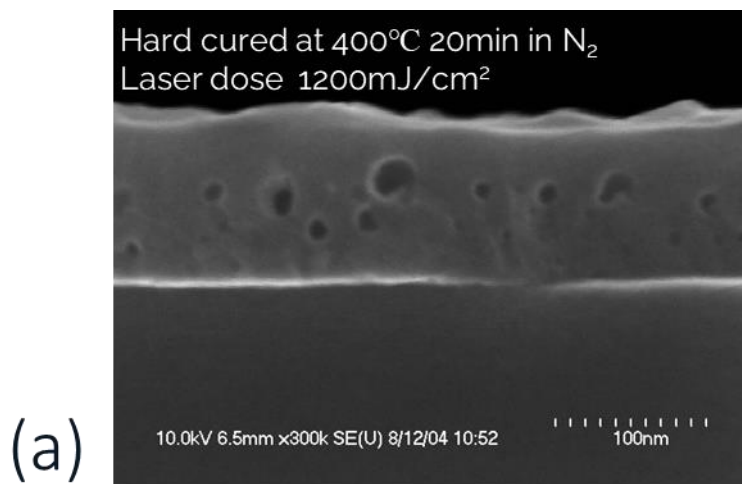


Figure 2.14: Cross-section SEM image of the excimer laser-annealed, spin-cast CPS film showing (a) film without the dehydrogenation bake, (b) film with the dehydrogenation bake, and (c) cross-section TEM image of crystallized island

To improve the wetness of the silicon ink, surface treatment was tested. Figure 2.15 shows the thickness at the center of 15 islands after hard baking, with, or without surface modification using HMDS and UV/ozone treatment. Figure 2.17 (a) and (b) shows a microscope image of the island with surface modification and a cross-section profile. The island had a smooth shape and surface.

Figure 2.17(c) and (d) show microscope images of the serrated island and a cross-section profile. The island formed a serrated shape, with spikes on the edge. The dome shape of the printed island caused the thin edges to be overdosed by the laser, which melted and pulled them back to form a serrated pattern. Figure 2.17 shows a microscope image after gate silicon was printed on a serrated island. The printed gate was broken from the edge, resulting in holes. The cross-sectional profile of the active island was optimized to prevent the formation of serrated edges by using surface modification.

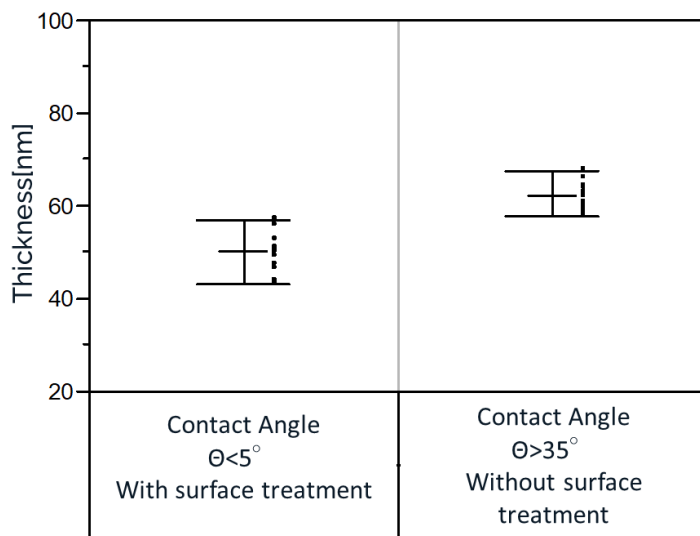


Figure 2.16: Thickness of the center of 15 islands after hard baking with or without surface modification

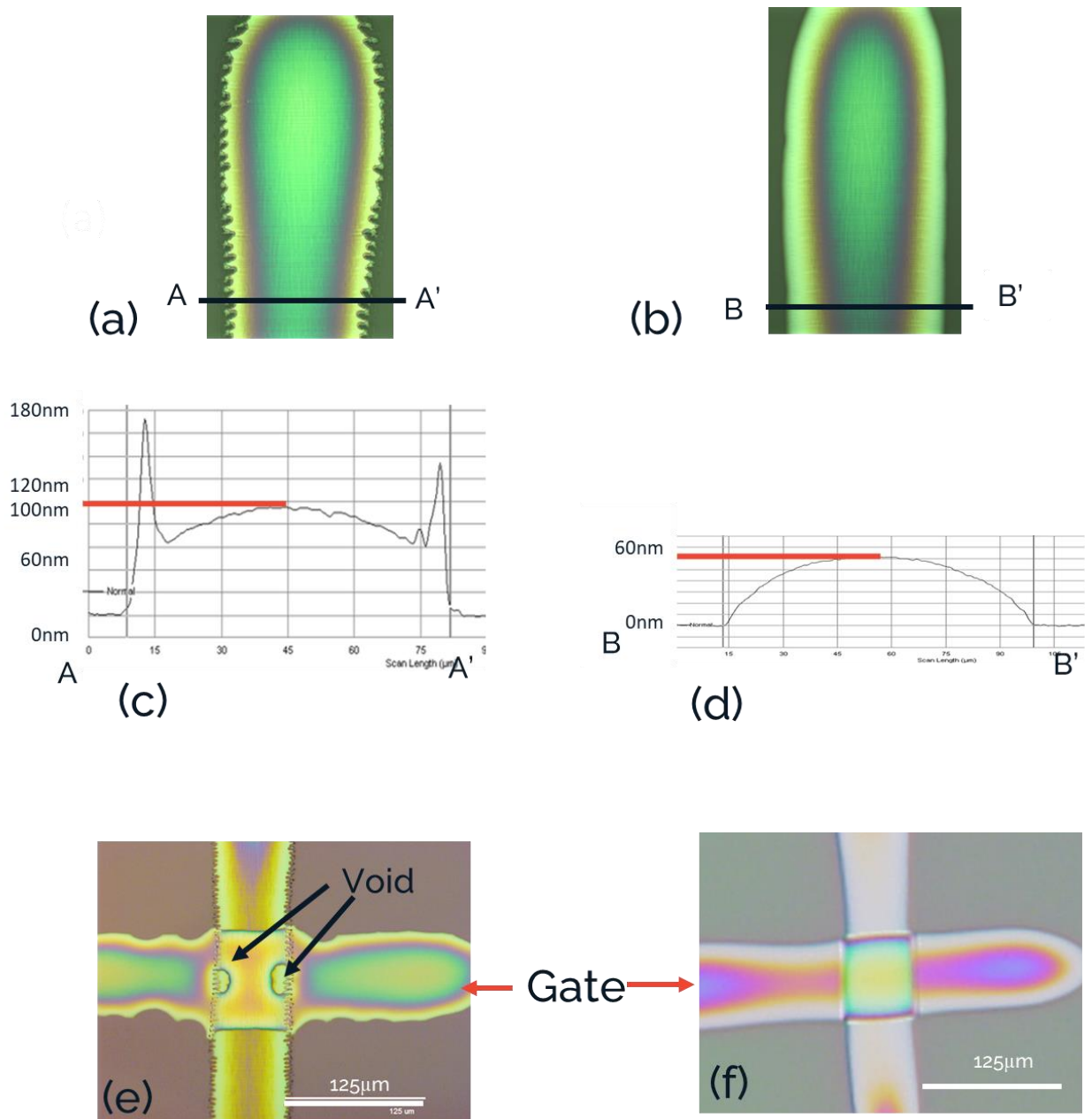


Figure 2.17: (a) A serrated shape of the printed silicon island without controlling after laser crystallization, (b) cross-section profiles of (a), (c) smooth-shape printed silicon active with CA control ($\theta < 5^\circ$) after the laser crystallization, and (d) cross-section profile. Printed gates (e) with a hole on top of the silicon island in the caterpillar shape, and (f) on top of the smooth island edge

Figure 2.18(a) shows a printed image of the neat B-30. The edge of the printed pattern was rolled and spread due to the self-induced Marangoni effect, as shown in Fig. 2.18(b). Figure 2.19 shows the P+ dopant ink formulated with B-30, diethylene glycol monobutylether, and surfactant on the active islands and gates. The P+ ink stayed in the printed area with good definition. Since the inkjet-printed P+ dopant lost its doping capability in air, the printing and soft-cure operations were performed in a glove box in ambient nitrogen. After thermal activation, the typical sheet resistance of the P+ doped silicon was $1 \text{ K}\Omega/\text{cm}^2$, while that of the N+ doped silicon was $300\text{--}500 \text{ }\Omega/\text{cm}^2$.

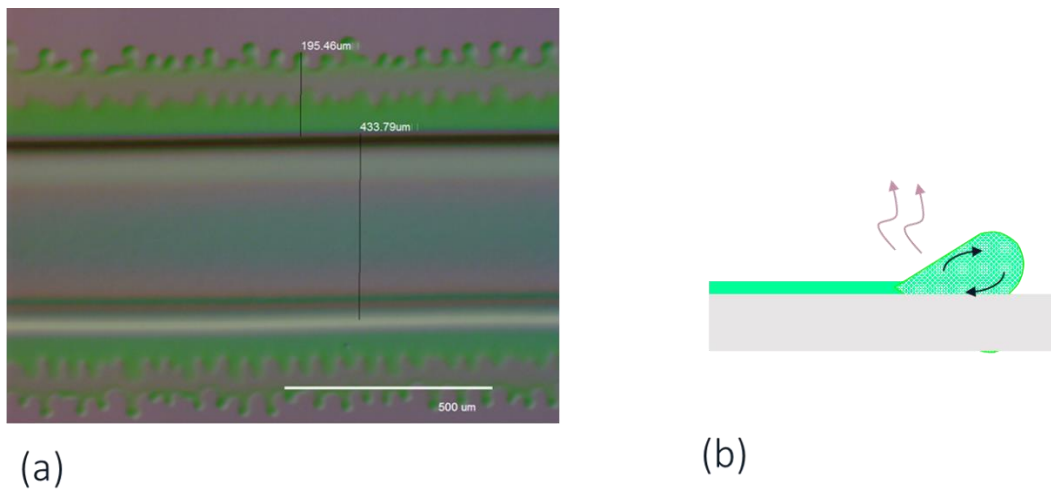


Figure 2. 19: Optical microscope images of (a) printed B-30 dopant base and (b) model of self-induced Marangoni flow

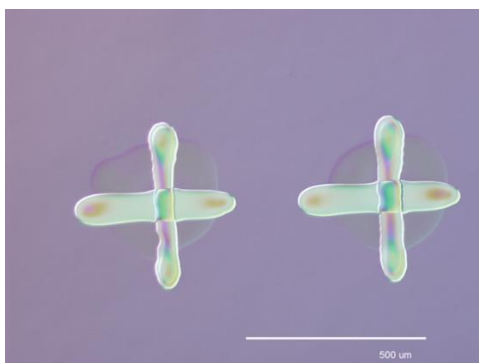


Figure 2.20: Optical microscope image of printed P+ ink on the active island and silicon gate

Figure 2.20(a) shows an SEM image of a palladium chloride ink printed on a silicon layer. Many small particles were observed. Figure 2.20(b) shows post-silicidation annealing. This suggests that under heat, the palladium chloride particles agglomerated and were then reduced and formed an alloy with silicon. The XRD spectrum of the palladium chloride inks that were spin-coated on silicon film after the silicidation anneal is shown in Figure 2.20(c). As evident in the phase diagram of the palladium-silicon system ^[20], the peaks at two theta values of 38.1°, 41.4°, 42.4°, and 48.5° were assigned to the reflection of (201), (210), (300), and (110) planes of hexagonal Pd₂Si, respectively. The ink with ethylene glycol showed a strong palladium peak compared with the ink with diethyl glycol butyl ether or a commercially available palladium precursor (Palladium Film, Emulsitone Company). Functional chains using Pd₂Si and aluminum interconnects were similarly demonstrated with contact resistances of approximately 10⁻⁶ Ω·m.

Fig. 2.21(a) shows a TEM image of the synthesized silver NPs. The approximate diameter was 5 nm in tight distribution. The finished silver NP and ink are shown in Figure 2.2(b). The sintering temperature must be significantly lower than the melting temperature of bulk silver. The melting temperature of bulk silver is 961.8 °C, and our silver ink was sintered at 280 °C, thus showing minimum resistivity. Figure 2.21(c) shows an SEM cross-sectional image of the sintered silver NP ink. The sintered ink revealed a dense grain structure. The formulated silver NP ink was extremely stable in day-to-day jetting compared with commercial inks, as it did not contaminate the nozzle plate. The typical resistivity of the heat-cured silver film was 10μ Ω·cm.

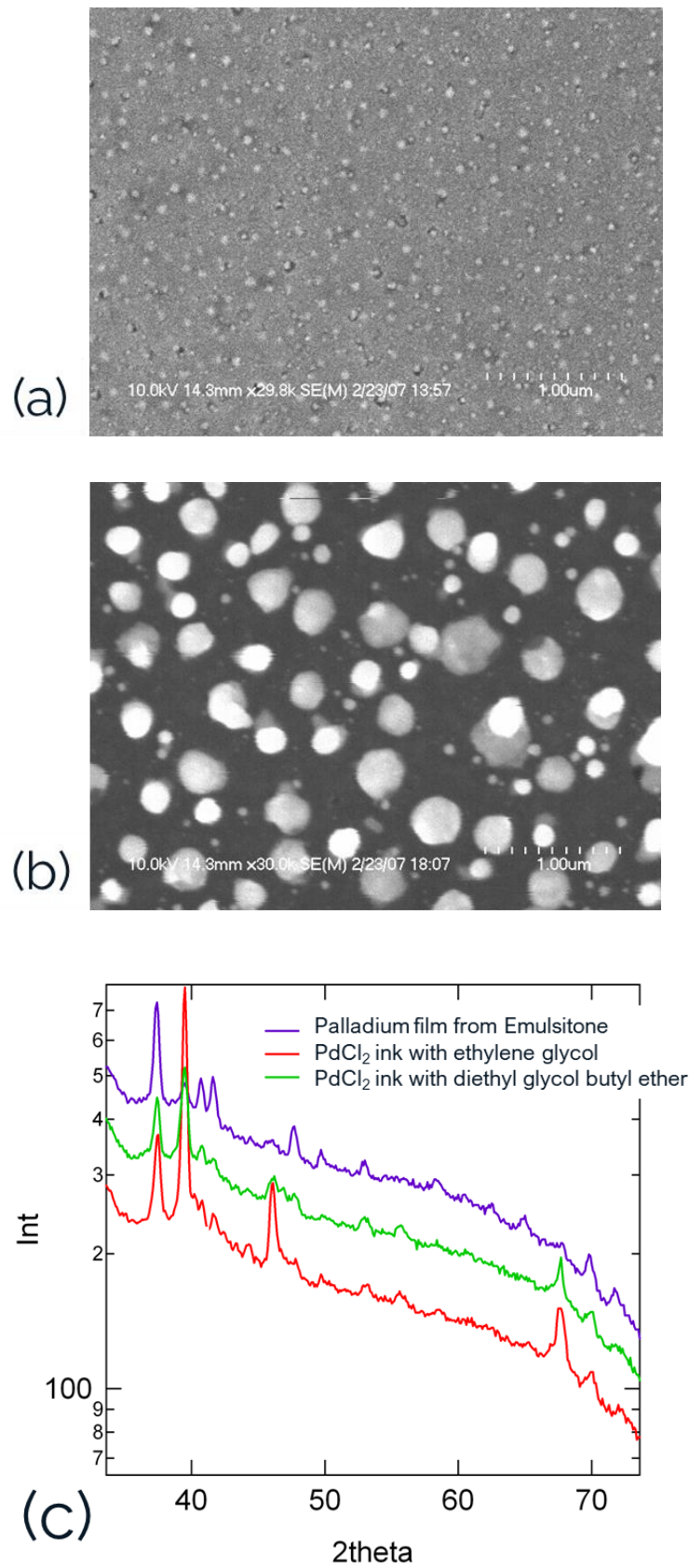


Figure 2.21: (a) Printed dopant on the silicon layer, (b) after silicidation anneal, and (c) XRD spectra of the spun palladium chloride ink after reduction in the forming gas

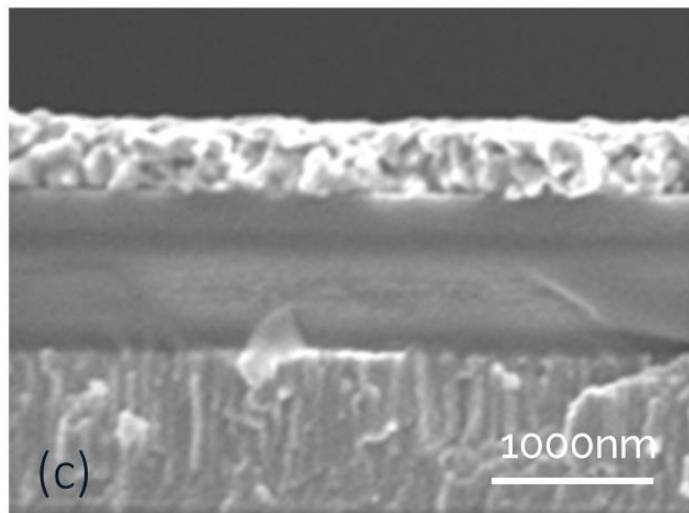
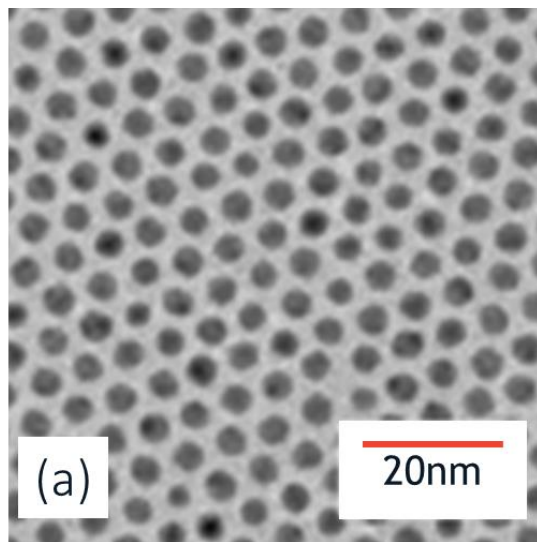


Figure 2.21: (a) TEM image of silver NPs, (b) photograph of silver NP and ink in cis-decalin, and (c) SEM cross-sectional image of heat-cured silver NP ink

3.2. TFT fabrication

All ink printing and annealing were integrated according to the diagram shown in Figure 2.11. Figure 2.23 shows an optical microscope image of an entirely inkjet-printed NMOS TFT. The yield of clean printing, as shown in Fig. 2.23, was not high due to misprinting caused by the clogged nozzle.

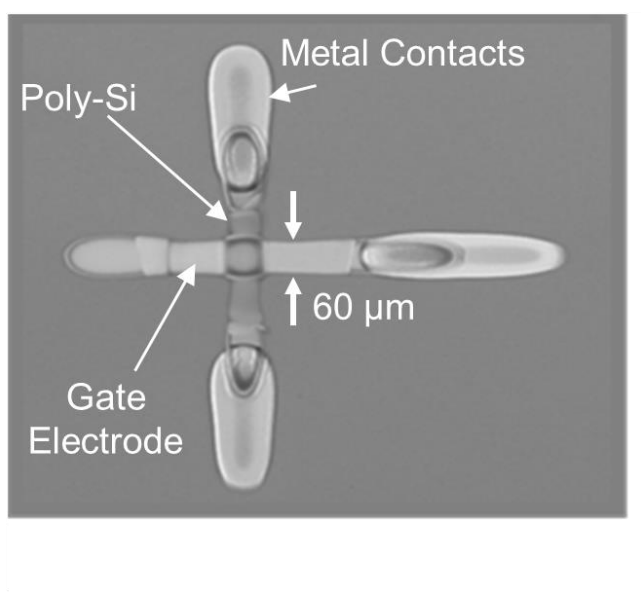


Figure 2.23: Optical microscope image of an entirely inkjet-printed NMOS TFT

4. Conclusion

In this study, a fabrication scheme for the first entirely inkjet-printed polysilicon TFTs was established using a unique set of newly developed inks. No ion implantation, vacuum deposition, or lithography techniques were used in any part of the process flow. Extremely low-impurity poly-CPS-based silicon ink was developed for inkjet printing. Cyclic hydrocarbon was chosen as the solvent to avoid contamination of the resulting silicon film. The dehydrogenation bake was optimized to avoid bubble formation during laser crystallization. To avoid a serrated edge of the island caused by laser irradiation on high-

profile islands, the profile of the island layer was kept low by surface modification of the field oxide surface before the printing islands.

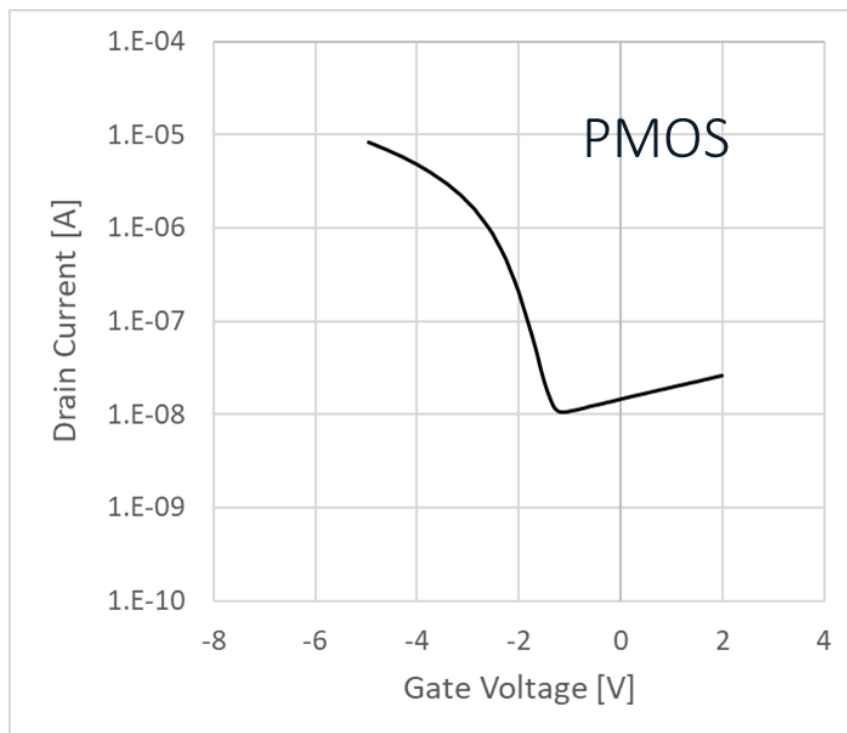
Dopant inks were formulated using spin-on-dopant as the base. The inks printed on the island were annealed and formed source and drain regions. The typical sheet resistance of the P+ doped silicon was $1 \text{ K}\Omega/\text{cm}^2$, while that of the N+ doped silicon was $300\text{--}500 \text{ }\Omega/\text{cm}^2$. Palladium chloride ink was developed to form silicide, which formed ohmic contact between the doped silicon and silver interconnection. The printed ink was reduced in the forming ambient gas, and silicide was successfully formed. The contact resistance to the silver layer was approximately $10^{-6} \text{ }\Omega\cdot\text{m}$. Using salt to form silicide is unique and consumes less material compared with evaporated or sputtered film or nanoparticle ink. The silver NPs were synthesized and formulated as inkjet ink. The ink showed good jetting stability, and the typical resistivity of the heat-cured silver film was $10\mu\Omega\cdot\text{cm}$. The future of printed electronics is promising. Since the completion of this study, -high frequency enabling gate lengths in the $1\text{--}10 \text{ }\mu\text{m}$ range have also been achieved using inkjet and other printing techniques ^[21, 22].

In the next step, the study addresses manufacturing issues in fabrication and yield, which need to be improved, as well as new developments in reducing capital cost and step count in manufacturing, thus enabling volume production. The multiple disadvantages of inkjet printing are also determined. First, the printing resolution was not fine enough to print a $4\text{-}\mu\text{m}$ dimension gate. Second, the printing reproducibility was not satisfactory, and the variability of the TFTs in a wafer was huge. Additionally, P+ doping ink lost the ability of doping with exposure to air, and both N+ and P+ inks left a glassy residue after activation, which damaged the gate oxide during residue removal. Based on these results, it was concluded that inkjet printing alone was not sufficient for the volume production of the logic circuit.

5. Appendix: TFT Characterization

CMOS TFTs were characterized using a KS-100 prober (Karl-Suss). Figure 2.24(a) and (b) show the drain current-gate voltage (I_d - V_g) curves of the best-performing TFT pairs. Because this was an early-stage study to determine proof of concept, device sample statistics were limited. The channel width was approximately 60 μm . The field-effect mobility of the NMOS TFT was determined to be $80 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The mobility of entirely printed polysilicon TFTs reached the range of the mobilities of common low-temperature polysilicon (LTPS) TFTs, which are fabricated using conventional vacuum deposition and lithography processes. The areas and mobilities of the typical good-performing NMOS TFTs were $50\text{--}110 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, while the mobility of the best PMOS was $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ (Table 2.4). The mobility and on/off ratios of the PMOS TFTs were worse than those of the NMOS TFTs. This results as attributed to the P+ dopant ink, which was more sensitive to the duration of exposure to air, as it degraded the doping capability, resulting in higher sheet resistance. For comparison, Table 2.5 shows TFT characteristics fabricated using other solution-based processes. The mobility of the entirely inkjet-printed polysilicon TFTs was significantly better than any of the other TFTs. High-performance CMOS TFTs with a mobility of more than $100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ were required to fabricate the logic circuit^[27]. This result demonstrated the future potential of printed electronics.

(a)



(b)

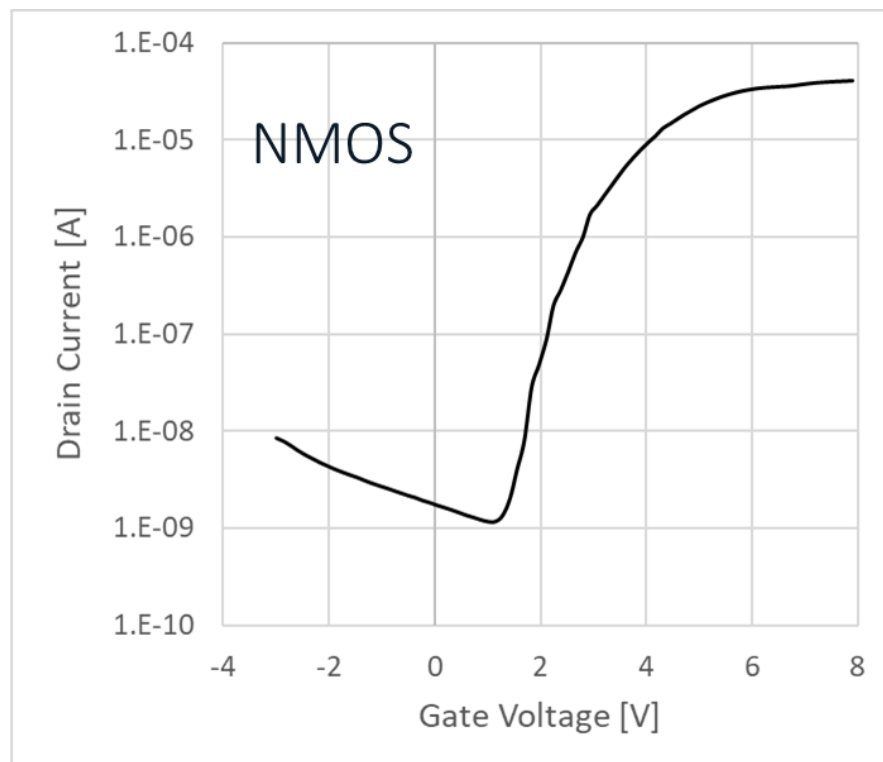


Figure 2.24: (a) I_d - V_g characteristics for the PMOS TFT, (b) NMOS TFT

Table 2.4: TFT properties of PMOS and NMOS for all inkjet-printed polysilicon TFTs

TFT Type	PMOS	NMOS
Mobility [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	14	110
Vt [V]	-2.3	2.3
Slope [V/dec]	0.68	0.58
ON/Off	0.7E+03	3/E+04

Table 2.5: TFT properties of TFTs fabricated from liquid-phase materials

Semiconductor film	precursor	Deposition technique	Mobility [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	Vt [V]	Slope [V/dec]	ON/OFF	Reference
Polysilicon	Poly-CPS	Inkjet/laser	110.0	2.30	0.58	3/E+04	This work
Polysilicon	Poly-CPS	Grain-filter/laser	597	1.7	0.21	1.7/E+8	[23]
Organic	DNTT	Inkjet	1.6	No data	No data	2.2/E+07	[24]
IGZO	Sol-gel	Spin	13.0	3.30	No data	1.7/E+04	[25]
CNT	CNT	Inkjet	37.7	No data	0.16	E+07	[26]

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Chapter 3

Study of Large, High-temperature Stainless Steel Foil Substrate

1. Introduction

1.1 Background

The direct fabrication of polysilicon TFTs on various flexible substrates has been widely investigated in the last decade. A variety of flexible substrates are commercially available for use in roll-to-roll processing. The key technical characteristics of a suitable substrate, including dimensional stability, flexibility, resistance to chemical attack, and non-permeability to water and oxygen, are compared in Table 3.1. Plastic films may be suitable for transparent and cost-sensitive applications, but they are prone to distortion and degradation at high temperatures. Dimensional stability requirements for tight layer-to-layer registration tolerances and high-temperature processing necessitate the use of metal alloys or stainless steel. Their ductility provides compatibility with subsequent dicing and assembly processes. In this study, to build a hybrid printing/conventional semiconductor development process, stainless steel foil was chosen as a substrate to build a hybrid printing/conventional semiconductor development process because of its flexibility, mechanical robustness, dimensional stability, heat resistance, and chemical resistance.

Table 3.1: Comparison of various flexible substrates

Parameter	Inorganic			Organic	
	Stainless (This work)	Alumina	Silicon	PET	Polyimide
Flexibility	Excellent	Poor	Poor	Excellent	Excellent
Brittleness	Excellent	Poor	Poor	Excellent	Excellent
High Temperature (°C)	1000	2000	1400	100	400
Thermal Conductivity (W/m°C)	260	15-38	168	0.24	0.29
Thermal Expansion (ppm/°C)	8.5	7	2.3	90000	30
Moisture resistance (g/m ² /24hr)	High	High	High	21	64
Oxygen Permeability cc/mm/m ² /hr/atm	None	None	None	0.12	0.37
Chemical Resistance	Excellent	Excellent	Excellent	Alkali	Alkali
Thickness (mm)	100	300	500	16-250	10-130
Cost (\$/m ²)	< 33		1100	5	13

1.2 Research objective

In this chapter, stainless steel foil and its treatment are studied to enable a hybrid printing/conventional semiconductor fabrication process that requires a high temperature process, dimensional stability for an overlay of 4 μm TFT, flatness for the optical process, and smoothness to minimize defects.

Regarding substrates, stainless steel foil is an attractive alternative for fabricating functional semiconductor components because it does not have the deficiencies of other substrates. Furthermore, stainless steel foil has several benefits, such as dimensional stability, mechanical robustness, flexibility, light weight, and a large area. It can also be processed at relatively high temperatures, which some processes require. It is also inert to most chemicals and is not permeable by moisture. These characteristics are ideal components of logic circuits, photovoltaics, sensors, and battery fabrication. Finally, the use of stainless steel enables roll-

to-roll processing, which allows for the high-volume, low-capital cost manufacturing of high-performance logic circuits in which high transistor density is not required.

The solar cell industry has used stainless steel foil in moderately high-temperature copper indium gallium diselenide (CIGS) processes. Dhere et al. demonstrated the fabrication of CIGS on a 20 μm thin stainless steel foil using a process temperature $< 475\text{ }^{\circ}\text{C}$ ^[1]. Kim et al. fabricated CIGS on 127 μm thin chrome steel ^[2]. Several efforts have been made to fabricate amorphous or polysilicon TFTs on stainless steel foil on a laboratory scale. Sekikawa and Omata fabricated high mobility polysilicon TFTs on stainless steel foil using sputtered amorphous silicon and implantation in a low temperature process at lower than $200\text{ }^{\circ}\text{C}$ ^[3]. Howell et al. and Wu et al. fabricated high temperature ($< 950\text{ }^{\circ}\text{C}$) polysilicon TFTs on 0.2 mm thick 304 stainless-steel ^[4,5].

However, several problems have been associated with fabricating devices on these substrates for volume production. The first is surface roughness, which can cause openings and shorts vertically and/or horizontally. CTEs of the steel alloy and stress relaxation after high-temperature processing are other major causes of concern in handling and precision layer overlaying. For example, the incoming foil flatness or warpage after high-temperature processing makes several processes, especially lithography or laser processing, difficult because it reduces the depth of its focus window. Dimensional stress relief (i.e., foil shrinkage) also matters in patterning multiple layers with a tight overlay because they become difficult to align. It is also difficult to prevent the diffusion of steel foil substrate metals such as iron and chromium (Fe, Cr) into active layers of a semiconductor device, which could otherwise cause several issues, such as leakage, breakdown voltage, and threshold voltage (V_t) control. Several researchers have addressed these issues. Hong et al. coated stainless steel foil substrates with spin-on-glass (SOG) and benzocyclobutane (BCB) to provide a smoother surface in fabricating amorphous silicon TFTs ^[6]. When the BCB was cured at a low temperature, and the SOG was cured at $600\text{ }^{\circ}\text{C}$, the results showed low leakage.

Yamada et al. used organic SOG to planarize a stainless-steel surface to demonstrate adhesion, chemical resistance, bending resistance, and electrical insulation^[7]. Troccoli et al. used SiO₂ as an insulator and encapsulation^[8].

Generally, substrates warp and cause problems if the stress level and shrinkage are not minimized. Consequently, optimization of the TFT fabrication process is critical to minimize this effect, especially when thin, flexible substrates large enough for volume manufacturing are used. Most previous research on TFT fabrication on stainless-steel foil substrates used sizes less than 150 mm². Furthermore, laboratory-scale production used plasma enhanced chemical vapor deposition (PECVD), laser crystallization, and ion implantation to keep the process temperature to a maximum of 650 °C.

NFC logic and sensor circuits were the initial target products of this research. To substitute for the high capital and maintenance cost of the ion implantation machine, screen printing was adopted, which also provided an advantageous pathway toward roll-to-roll capability^[12]. Screen printing is a mature technology, the maintenance and capital of which cost a magnitude order lower than conventional semiconductor processes. However, the activation process for screen printing requires an annealing temperature > 800 °C. Neither SOG nor BCB coatings can support these thermal budgets because of cracking or delamination. Furthermore, at this temperature, trace metals diffuse into thin layers of SiO₂. Moreover, most foils tend to suffer irrecoverable plastic deformation. However, other substrates that can withstand these temperatures, such as flexible ceramic or quartz, are expensive and brittle, and alternative low temperature processes sacrifice TFT performance. Because of all these characteristics, stainless steel foil is an attractive alternative.

In this study, a low CTE 300 mm² stainless steel-foil substrate with excellent smoothness and flatness was developed. To prevent trace metal diffusion from the substrate into the silicon active layer, a novel encapsulation and insulation layer combined with a diffusion barrier layer was developed. Process control was a key integration requirement.

Common stainless steel 304 has a CTE greater than 17 ppm/°C. However, to achieve an overlay of 4/8 μm TFT across a 300 mm² substrate, the CTE should be less than 10 ppm/°C. Therefore, alloys with an appropriate composition (e.g., low nickel content) were selected. This steel foil substrate then needed to be polished using a combination of mechanical and chemical methods, first to reduce defects that can potentially cause shorts and second to impart a mirror-like finish with high reflectivity to allow for wide laser and lithography process windows. Substrate surface flatness was also critical because the depth of focus required for lithography and laser annealing to crystalize silicon necessitates that it typically be less than 20 μm . Therefore, the pre-annealing temperature was optimized to relieve stress and maximize flatness to meet the required optical process in a wide window. Because the defectivity of the surface was also affected by polishing and annealing, the process results were evaluated both optically and electrically. To allow for high-temperature processing, the stainless steel foils also had to be completely pre-encapsulated to prevent substrate oxidation during annealing. Polysilicon CMOS TFTs were then fabricated on 300 mm² substrates using four lithography layers with a +/-2 μm overlay. Table 3.2 is the summary of specification required.

Table 3.2 Required specifications for the stainless steel foil substrate

Items	Specification
Roughness	Ra< 2nm
Defect	Minimum
Flatness	< 20 μm
Thermal expansion	<10ppm/°C
Warping/flatness	<20 μm
Trace metal diffusion	1E+16
Dimension stability	< +/- 2 μm

2. Experiments

A stainless-steel alloy with a low coefficient of thermal expansion < 10 ppm at 0–800 °C was chosen as a substrate. The foils were pre-annealed at three temperatures. Figure 3.1(a) shows “I” units, which indicate that flatness was evaluated using the results of optical 3D measurements across a 300 mm² sheet. The I-unit is an exacting quantitative flatness measurement and the industry standard for determining the flatness contained in ASTM A1030. It is a dimensionless number that incorporates both height (H) and peak-to-peak length (L in the following formula):

$$I = \left[\frac{3.1215 * H}{2L} \right]^2 * 10^5$$

The foil was polished for surface planarization. Surface morphologies were measured using atomic force microscopy (AFM). Defectivity in the vertical and horizontal directions of the foil surface was evaluated using the following methods: Fabrication of 24000 metal insulator metal (MIM) capacitance structures shown in Figure 3.1(b) were used to capture the level of vertical defects, such as metal “spikes” that could cause shorting by piercing through barrier and insulator layers. Horizontal defectivities, such as metal hillocks or valleys, which could negatively affect lithography causing horizontal bridging between metal or active structures causing shorts, were evaluated by fabricated interdigitated fingers with 4 μm/4 μm line and space. Figure 3.1(c) shows a microscope image of the interdigitated fingers.

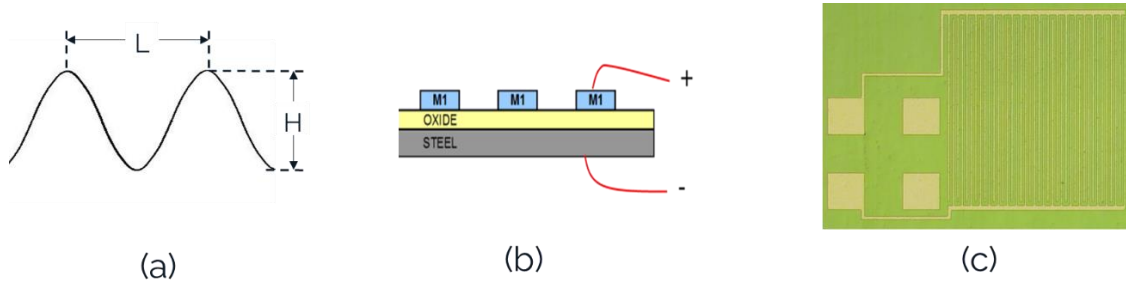


Figure 3.1: (a) Description of I unit, which indicates flatness, (b) MIM capacitor fabricated on stainless steel foil, (c) interdigitated comb structure

The complete encapsulation was deposited on the stainless-steel foil substrates after wet cleaning to degrease and remove contamination from the foil surface. A proprietary thin barrier layer was first deposited, followed by a thermal insulator layer to enable laser processing compatibility. Multiple combinations of barrier and insulator layers were tested. After deposition of the barrier and insulator layers, the foils were annealed at temperatures above 800 °C to release stress and preshrink the substrate. This is the highest temperature process used to fabricate polysilicon TFTs. To measure diffusion barrier properties, high-precision SIMS depth profiles were taken to measure the movement of trace metals from the substrate toward the active layer. Typically, the primary concern with metals is the high diffusivity of Cr compared with Fe or Ni. After the annealing process, flatness was tested using a vacuum chuck.

3. Results and discussion

A 3D optical image and associated I unit, which indicate the flatness of the foil substrates with three different pre-annealing temperatures, is shown in Fig. 3.2. Bumps at edges decreased in the lower pre-annealing conditions, and the associated I unit was minimized to $I_{max} = 2$. Figure 3.3(a) and (b) show the AFM profile before and after mirror polishing of the stainless-steel foil. The arithmetic average roughness (Ra) after polishing was less than 2 nm.

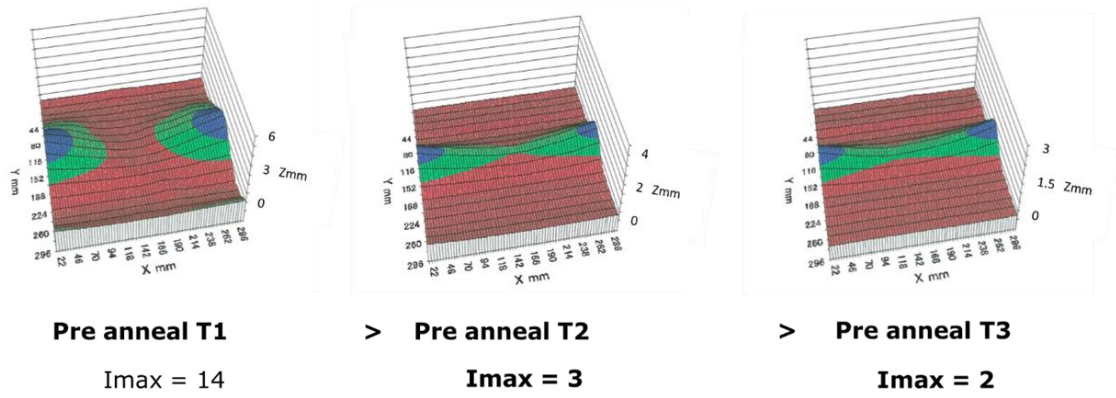


Figure 3.2: 3D measurement profile and Imax of 300 mm² stainless steel anneal at three different temperatures

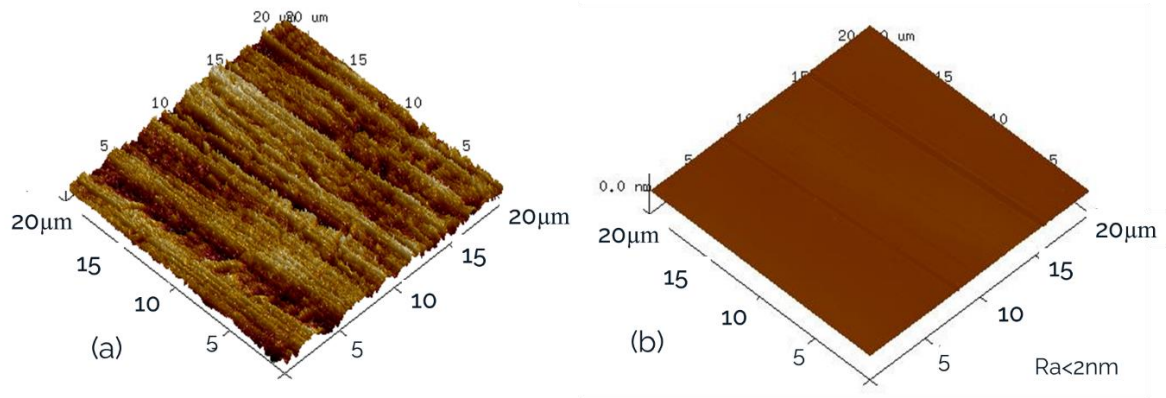


Figure 3.3: (a) AFM profile of surface stainless steel foil without polishing, (b) AFM profile of surface stainless steel foil after mirror polishing

The defectivity of the surface was alleviated by polishing and annealing. Figure 3.4(a) and (b) show microscope images of the surface of the stainless-steel foil after proprietary polishing and annealing, as condition 1 and condition 2. The surface of the foil treated under condition 2 had fewer defects and fewer bumps. Under condition 2, the vertical defect density was minimized at 0.01 /cm². Figure 3.4(c) shows the yield map of the capacitors. The shorted dies are shown in red.

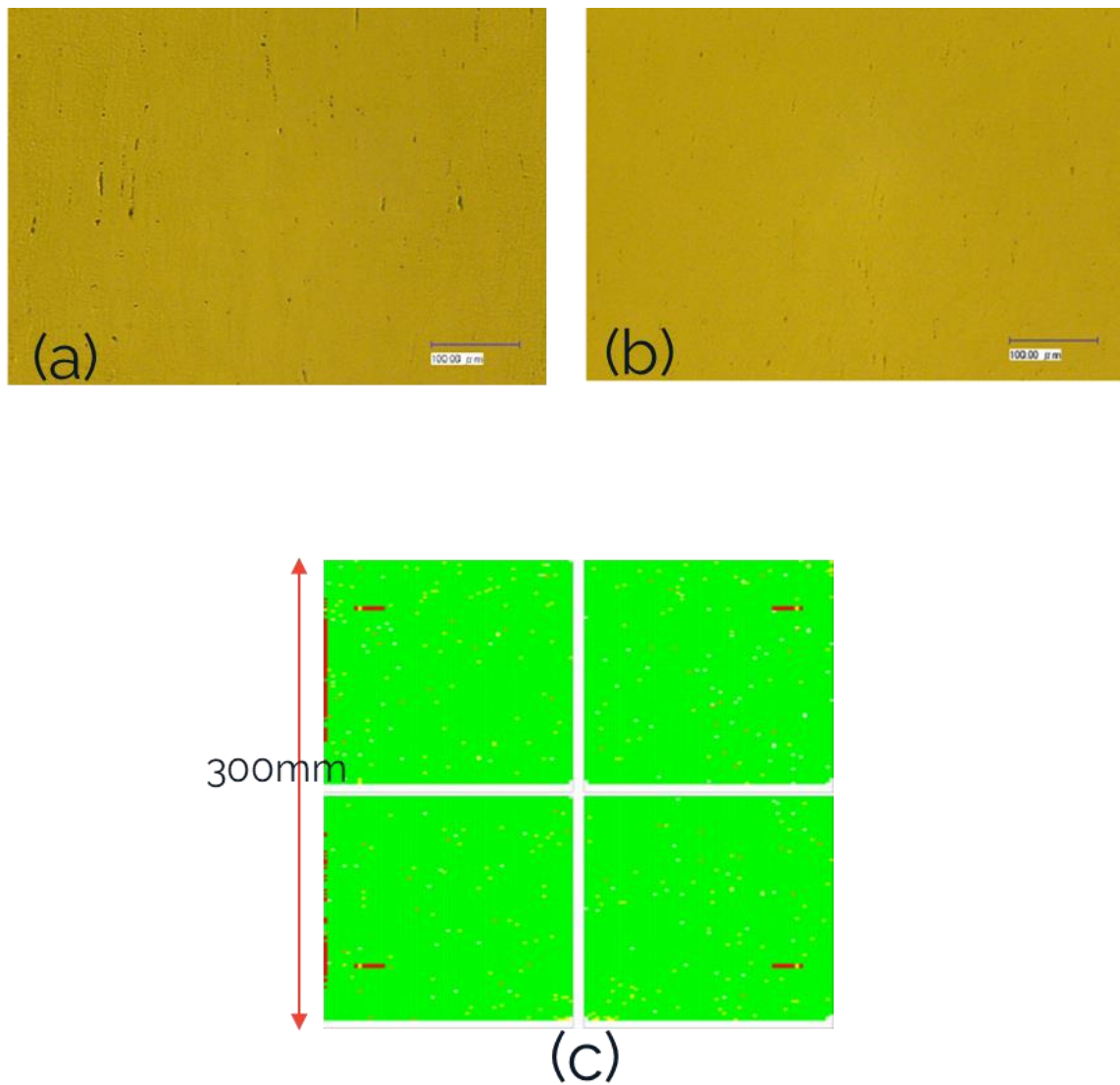


Figure 3.4: (a) Microscope picture of foil surface polished and annealed with condition one, (b) microscope picture of foil surface polished and annealed with condition 2, and (c) yield map of MIM capacitor. The dies shown in red were shorted.

Horizontal defectivity was evaluated by interdigitated fingers, and all shorting defects were investigated using an optical microscope. No shorts were caused by steel defects in 240 combs across the 300 mm² foil. Figure 3.5 (a) shows the flat stainless steel foil substrate after optimized post-encapsulation annealing, and Figure 3.5 (b) shows that the warped stainless steel foil substrate without optimization of annealing was not sucked down on the vacuum chuck.

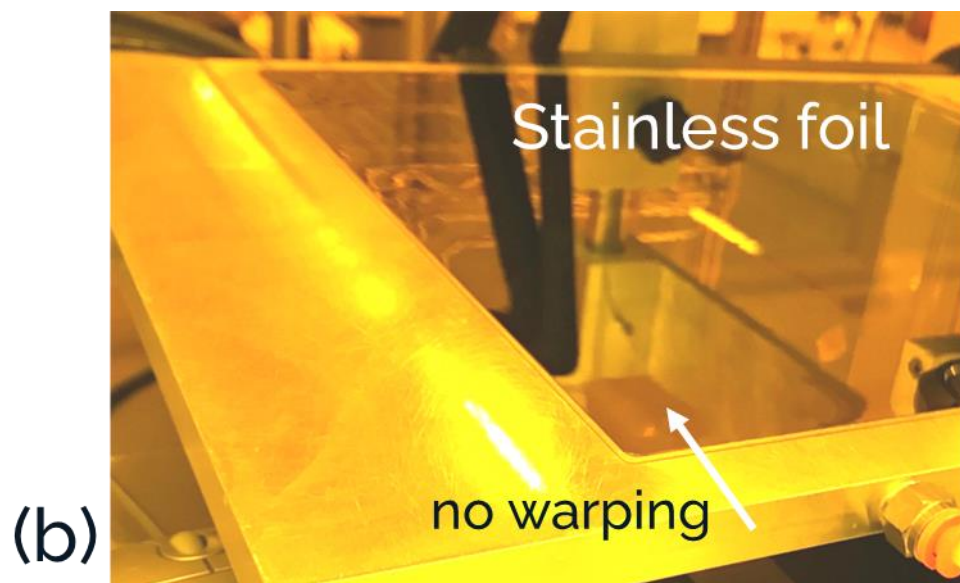
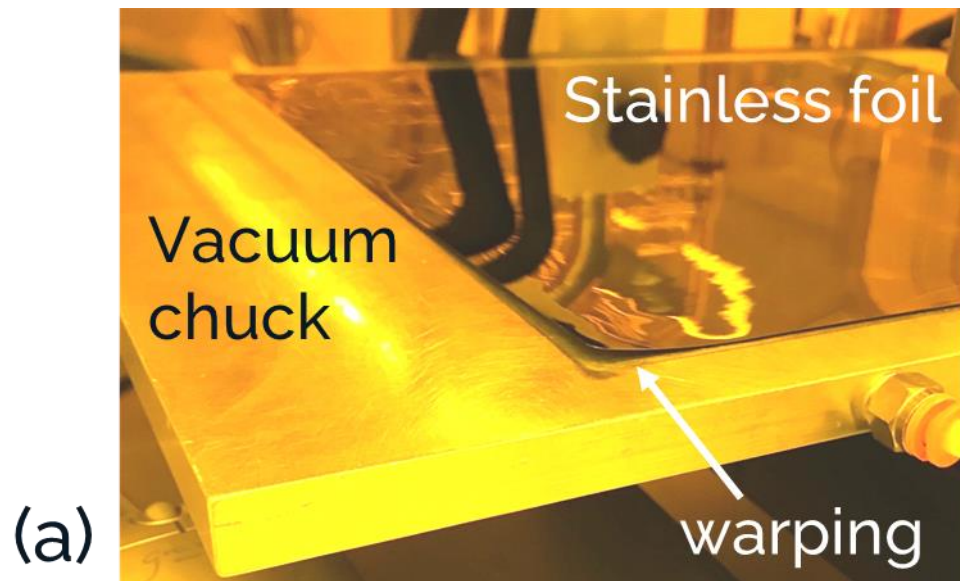
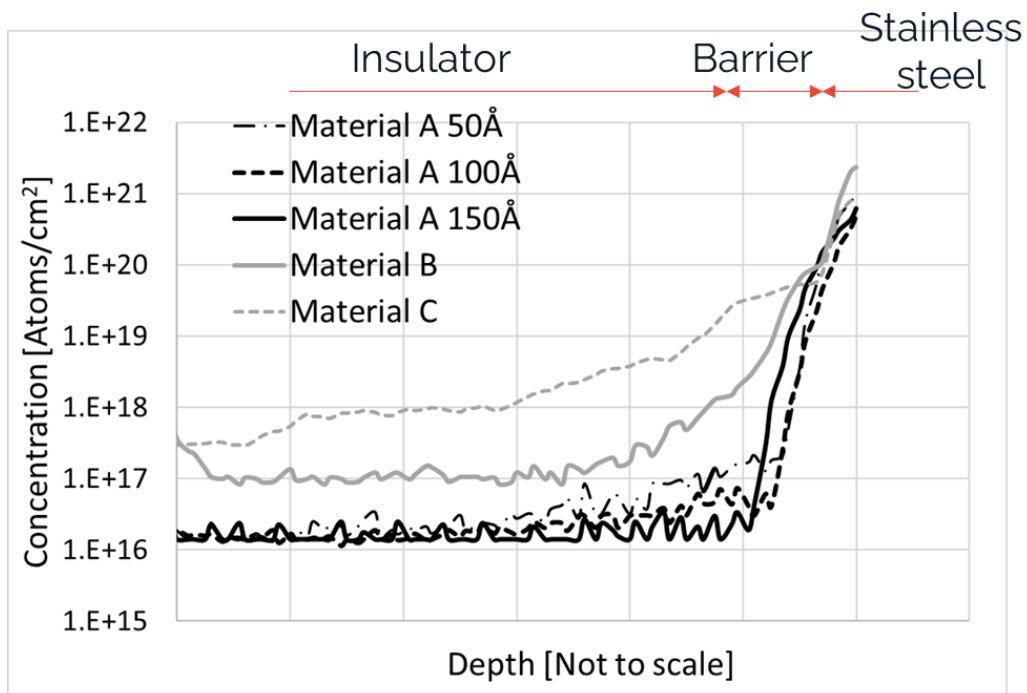
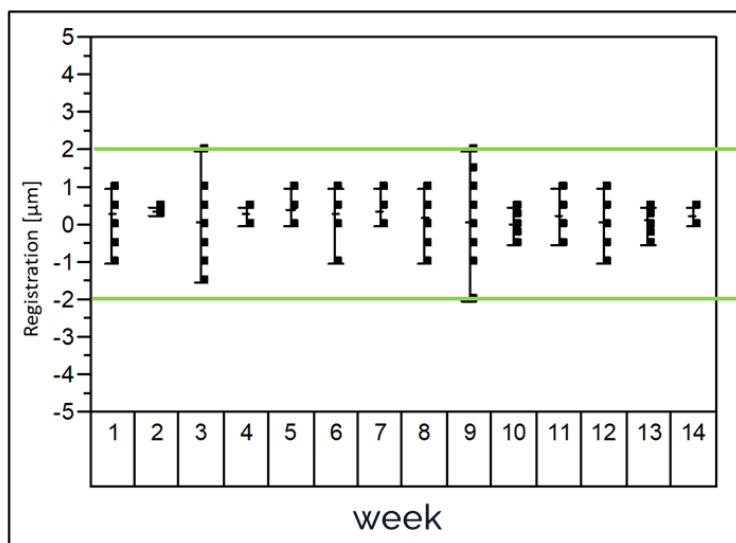


Figure 3.5: (a) Flat stainless steel foil substrate after optimized post encapsulation annealing, (b) warped stainless steel foil substrate after annealing without optimization was not sucked down on the vacuum chuck

After deposition and annealing of the barrier, SIMS depth profiles were taken to measure chromium. Figure 3.6(a) shows that the chosen barrier layer (Material A, thickness 3) effectively stopped the diffusion of chromium into the insulator. Figure 3.6(b) shows the registration accuracy between the gate and interlayer dielectric (ILD) layers measured daily in the manufacturing environment. The registrations of the ILD layer were consistently less than $\pm 2 \mu\text{m}$ across the 300 mm sheets, even after the thermal annealing process, which was done sequentially between the gate and ILD layering. The dimensional stability of the stainless steel foil was proven adequate to manufacture $4/8 \mu\text{m}$ TFT circuits using a thermal annealing process above 800°C .



(a)



(b)

Figure 3.6: (a) Post-high temperature annealing SIMS relative depth profile of Cr through various diffusion barriers, (b) gate-ILD registration across 300 mm sheet over 14 manufacturing weeks

4. Conclusion

A large area stainless-steel foil substrate compatible with high temperature ($> 800\text{ }^{\circ}\text{C}$) processing was investigated to support a hybrid printed and conventional semiconductor process technology for the fabrication of polysilicon TFTs. The use of stainless steel as a substrate over alternative materials was chosen because it offers multiple benefits. First, it can withstand high-temperature processing, which enabled the adoption of screen printing that eliminated the need for high cost, high maintenance ion implantation. Second, it does not require expensive back-grinding for thinning or a precision attach process. It is mechanically robust and offers dimensional stability. It also offers extreme flexibility, light weight, and a large area. It is inert to most chemicals and exhibits no moisture permeability. Finally, it promises roll-to-roll processing, leading to a very high volume and low CO_2 emission manufacturing.

A stainless steel foil substrate based on a low thermal expansion coefficient alloy was selected and optimized to minimize defectivity and maximize flatness. The fabrication process was optimized to avoid issues arising from the use of stainless steel at high temperatures, such as bowing and diffusion of trace metals. A volume production pilot line using a large-area substrate in a manufacturing environment was demonstrated. Fabricated tags and NFC circuits were readable with a smartphone at a range of several cm. This stainless steel foil substrate was compatible with a high-temperature fabrication process, which has the potential for a variety of applications, such as photovoltaic, sensor, and battery fabrication that requires a high-temperature process on a large area flexible substrate.

5. References

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Chapter 4

Slot-die Coating of Silicon Ink

1. Introduction

1.1. Research objective

In Chapter 1, CPS-based silicon ink was shown to be promising for forming the polysilicon layer in high performance TFTs ^[1]. However, inkjet and other printing techniques could not meet the resolution and reproducibility required to move from the laboratory to an active island 4 μm wide pilot line for volume production. To move the printing process forward more rapidly, instead of layering via inkjet, a poly-CPS ink was slot-die coated to form a PECVD equivalent silicon layer. This combination is the focus of this chapter.

In this study, both a monomer CPS ink and a poly-CPS ink were simultaneously formulated for comparison and developed as precursors of silicon film for comparison purposes. First, the ink formulation was optimized for a high-throughput large-area uniform slot-die coating. In general, in air drying a polymer solution coating film, if only a high boiling point solvent is used, then it takes a long time to dry, during which “mura” caused by the Marangoni flow or “dripping” caused by gravity occur. However, if only a low boiling point solvent is used, then defects such as “orange peeling” or “pin holing” due to rapid evaporation occur. In either case, it would be difficult to form a smooth dense film ^[2,3]. Hence, to formulate poly-CPS inks, a cosolvent (cyclohexane/cyclooctane = 95/5) was used to suppress the haze defect, which appeared when only cyclohexane was used.

In laser crystallization, silicon film enabled the production of high-mobility polysilicon CMOS TFTs in a manufacturing environment. In the crystallization process, a solid-state

green (532 nm) laser ^[4-6] was chosen. The benefits of using the green laser were the absence of halogen gas, low energy consumption, stability, and compactness. Unlike display applications, small beam sizes are not an issue in the application of logic circuits. Additionally, because 532 nm can be absorbed by polysilicon, a novel process, such as laser doping, was expected.

The slot-die coater was developed to coat a 300 mm² substrate in an inert environment and integrated in a glove box with a UV lamp house to simultaneously irradiate the coated silicon film. This combination provided for large-area manufacturing at high speed and economizing on ink.

1.2. Slot-die coating

The slot-die coating technique is used in the application of solution, slurry, or extruded thin films onto smooth substrates, such as metal foils, plastic films, and glass plates. The process was first developed for the industrial production of photographic films in the 1950s ^[7]. Since then, it has been used to deposit a variety of liquid chemistries onto roll-to-roll for the development and production of a broad range of applications. In the early 1990s, slot-die coating technology was developed to dispense on a flatbed substrate, which allowed for efficient, high-performance spinless coating in applications such as flat panel displays to coat photoresist, color filter materials, organic light-emitting diodes ^[8], photovoltaics ^[9], solid state lighting, and various organic and printed electronic applications such as RFID, polymer batteries ^[10], and sensors ^[11-13].

The coating materials were dispensed onto the surface of the substrate through a slot-die nozzle that was designed and machined precisely. The width of the coating was determined by the dimensions of the nozzle outlet, and the coating length was controlled by an on/off pump. Finally, the coating thickness was controlled by the rate of solution deposition and the

relative transfer speed of the substrate. Therefore, slot-die coating afforded thin material coatings with easily controllable dry thicknesses ranging from 10 to several 100 nanometers.

Thus, the benefits of the slot-die coating process were determined to be its pre-metered control of thickness, throughput speeds, non-contact coating mechanism, high material efficiency, scalability of coating areas and throughput speeds, and roll-to-roll compatibility. The process also allowed for a wide working range of layer thicknesses and precursor solution properties, such as material choice, viscosity, and solid content. Its closed system and non-contact coating aspect was the major advantage for silicon ink coating. The disadvantage of the slot-die coating process was the comparatively high complexity of the apparatus used to maintain coating quality, such as nozzle cleanliness, nozzle assembly, gap control, and process optimization, compared with other coating techniques, such as spin coating.

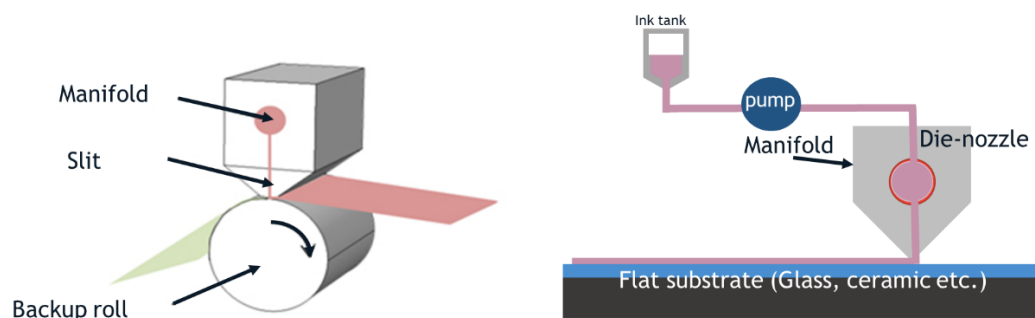


Figure 4.1: Slot-die coating on (a) roll-to-roll web and (b) flatbed coat substrate

2. Experiments

2.1. Ink formulation

Poly-CPS, which was described in Chapter 2 and shown in Figure 4.2, was used to formulate ink for the slot-die coating. In this study, a wire-bar coating on 4-inch silicon wafers with simultaneous UV irradiation was used to screen the ink formulation. Figure 4.3 shows wire-bar coated and hard baked poly-CPS films formed using various ink formulations. When cyclooctane was 100%, film thickness variations due to the Marangoni effect were obvious. However, the film thickness was improved by increasing the amount of cyclohexane. The solvent ratio of cyclohexane/cyclooctane was determined to be 95/5, which showed good uniformity of film thickness although a pin hole was observed.

CPS and poly-CPS were separately dissolved at 4 wt% in cyclohexane/cyclooctane (95/5 vol%) to prepare them for extrusion coating. The inks were developed for volume production. Therefore, the specification of the shelf life was -20 °C for two months, and the bottle life was at room temperature for seven days. CPS and poly-CPS inks with a molecular weight of approximately $M_n = 1000$ were both stable under these conditions. The poly-CPS ink, with its larger molecular weight, showed precipitation with the condition of shelf life and bottle life. The cyclohexane and cyclooctane ($\geq 99\%$, Sigma Aldrich) were first washed with sulfuric acid ($\geq 95\%$, Sigma Aldrich), and then washed with water to remove any peroxide and oxygen compounds that could potentially contaminate the silicon film and reduce carrier mobility. They were then distilled over sodium ($\geq 99.8\%$, Sigma Aldrich) to remove the water.

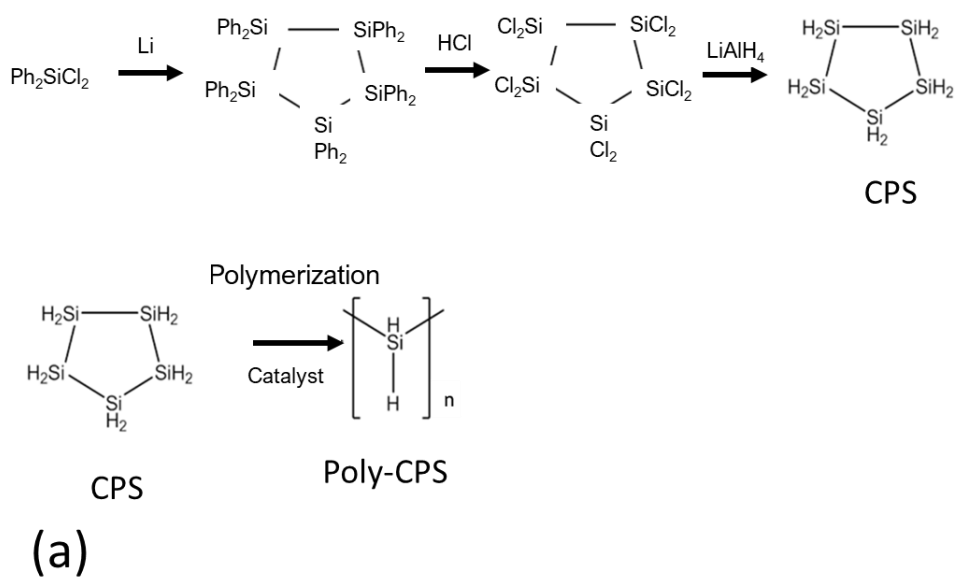


Figure 4.2: (a) Synthesis path of cyclopentasilane and CPS polymerization using a catalyst, (b) GPC spectrum of CPS and poly-CPS

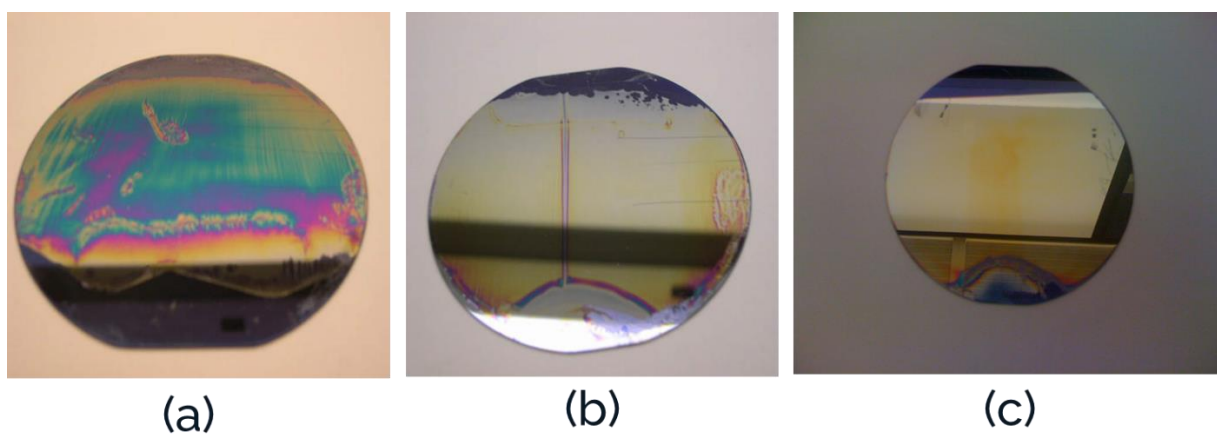


Figure 4.3: Poly-CPS formulated with various solvents, coated using wire bar, UV irradiated simultaneously then hard baked (a) cyclooctane 100 vol%, (b) cyclohexane/cyclooctane (95/5 vol%), and (c) cyclohexane (100 vol%)

2.2. Slot-die coater setup

Figure 4.4(a) provides an overview of the slot-die coater and the hot plate setup in their respective glove boxes. The three glove boxes with individual circulation systems were combined and separated by a shutter door. Figure 4.4(b) shows the front views of the three glove boxes. The ambient in the slot-die coater box was maintained at room temperature, while the hot plate box ambient became hotter due to the hotplate. Stainless steel foil substrates were loaded from the left antechamber, placed on the granite chuck, and coated with silicon ink on the slot-die coater. After coating, the sheet was lifted from the granite chuck and transferred using a manual fork via the shutter door to the hot plate box. The sheet was then baked on the hot plate and finally unloaded via the right antechamber.

Figure 4.5 shows a schematic of the slot-die coater. The CPS and poly-CPS ink films were dispensed on a 300 mm² stainless steel foil substrate using a slot-die nozzle, as shown in Figure 4.6(a). The slot-die nozzle was 350 mm wide with a 290 mm dispense width. It was integrated in tandem with a UV lamp house. UV light was attached directly behind the nozzle, as shown in Fig. 4.6(b), to simultaneously irradiate the films. Because CPS and poly-CPS are pyrophoric and oxidize in contact with oxygen, the slot-die coater (nTact extrusion-coater) was integrated into a Mbraun glove box with inert nitrogen gas. A low-pressure mercury grid lamp was chosen for UV irradiation because it generated less heat, which eased temperature management during manufacturing. A sliding shutter made of polyimide film was integrated with the lamp house to control the on/off of UV irradiation. To maintain the lamp's temperature in the operating range, the lamp house was subjected to a continuous flow of nitrogen gas. Finally, the exhaust valve was linked to the shutter switch. When the shutter was opened, the exhaust valve then opened. A positive displacement pump using a glass syringe was adapted to pump ink into and provide consistent flow from the nozzle. To avoid carbon or metal contamination, all parts in contact with the inks were made of glass, stainless steel, polytetrafluoroethylene (PTFE), perfluoro alkoxy (PFA), or polyether ether

ketone (PEEK). Oxygen and H₂O levels were controlled < 5 ppm to prevent oxygen from contaminating the coated film.

Because stainless steel foil sheets warp with heat, the equipment used to heat the silicon wafers could not be used in this study. For example, a stainless-steel foil on a typical hotplate warped badly, as shown in Fig. 4.7(a). Because of the warping thermocouples in a rapid thermal annealing (RTA) tool, it would not be able to monitor and control the temperature.

Therefore, a newly designed hotplate was integrated into the glovebox for hard baking above 400 °C. As shown in Fig. 4.7(b), the design prevented warping integrated proximity pins that provided radiated heat instead of contact heat, and a clam shell lid on the exhaust maintained the temperature even throughout this process. Temperatures at five points across the stainless steel foil substrate were measured by K-type thermocouples stapled on the substrate. The hot plate turned the soft polymer film into amorphous silicon ^[19].

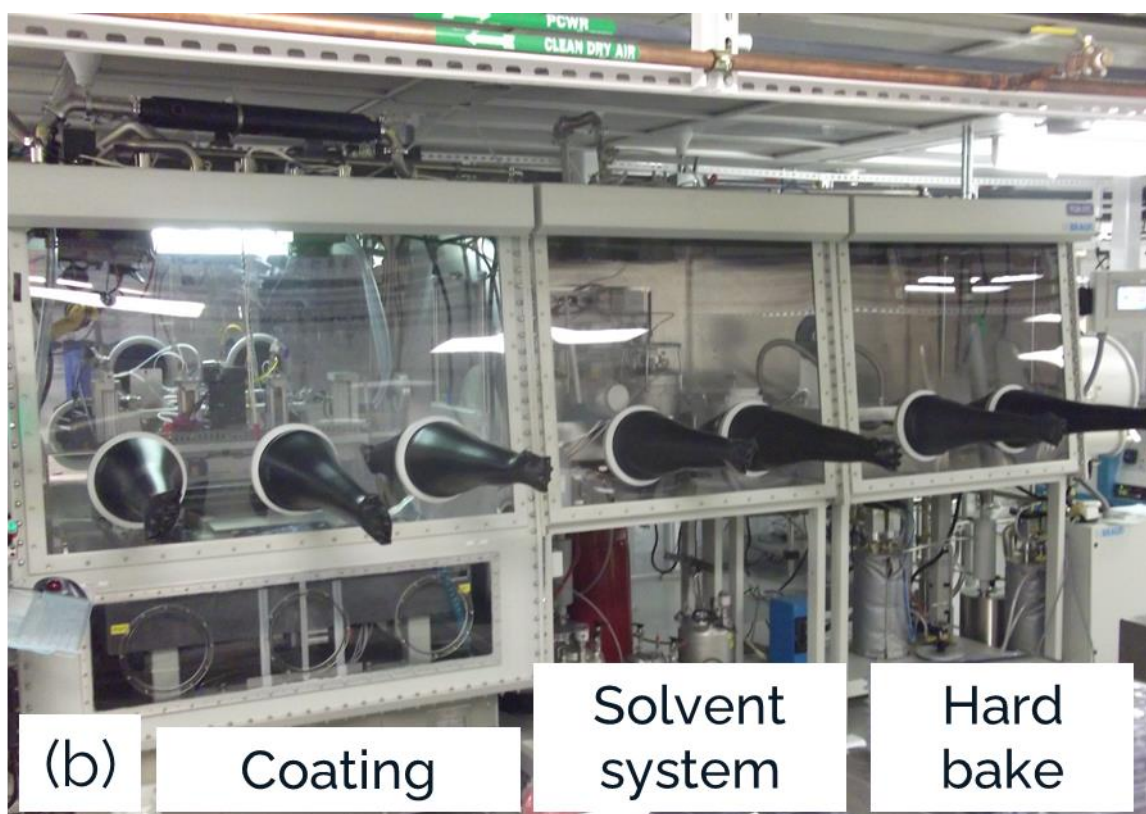
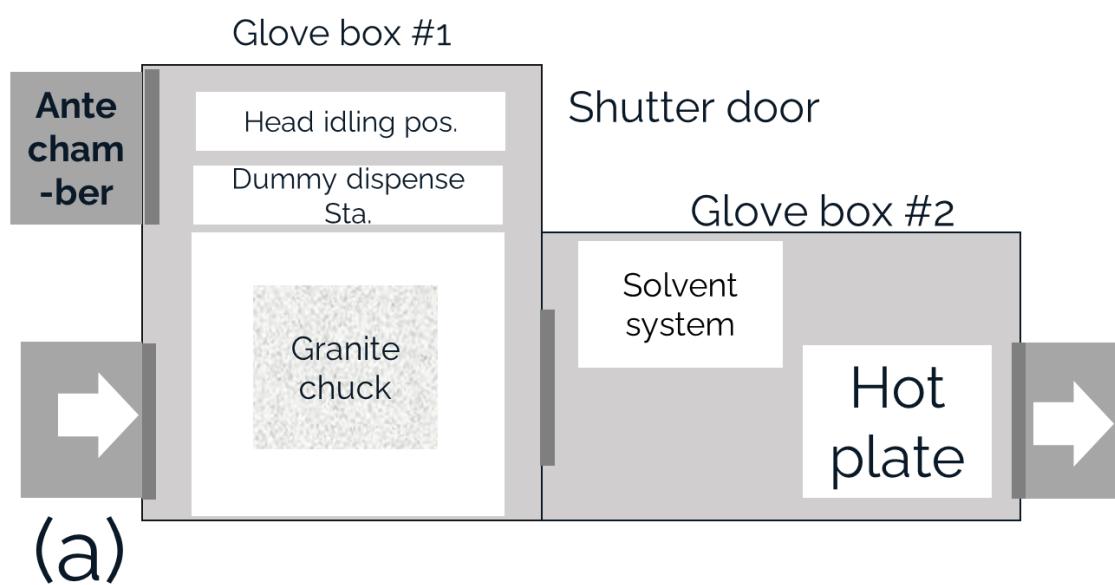


Figure 4.4: (a) Overview of the slot-die coater and the hot plate in the glove boxes combined via the door shutter, (b) photograph of the glove box and coater

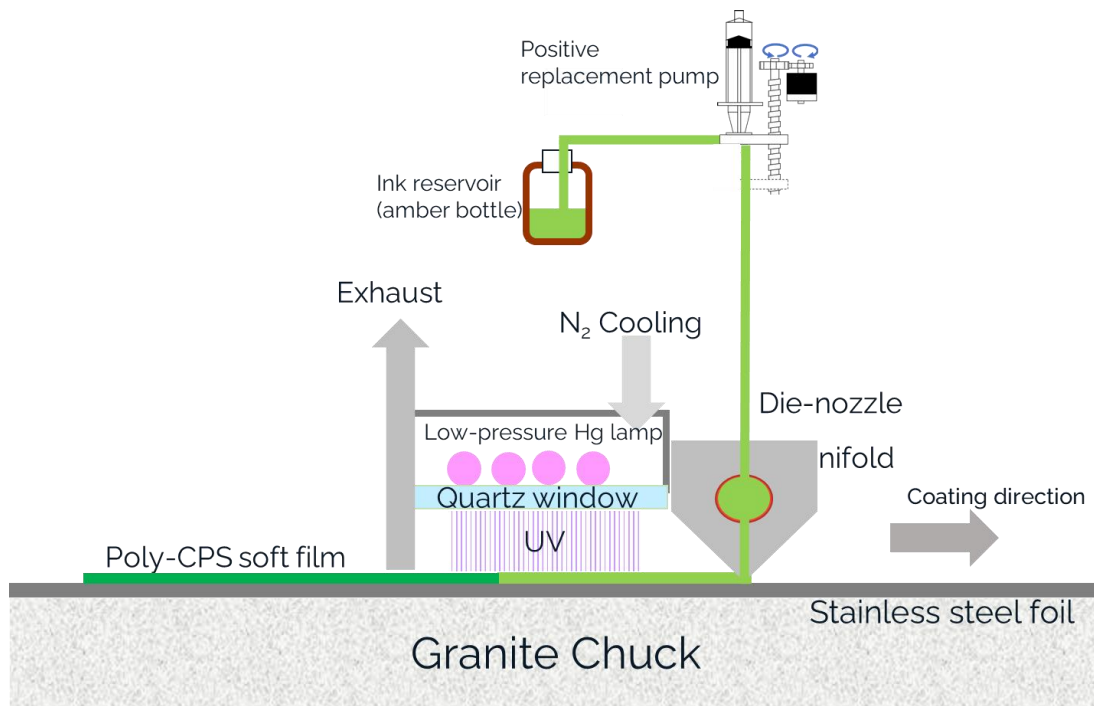


Figure 4.5: Process diagram of the slot-die coating setup

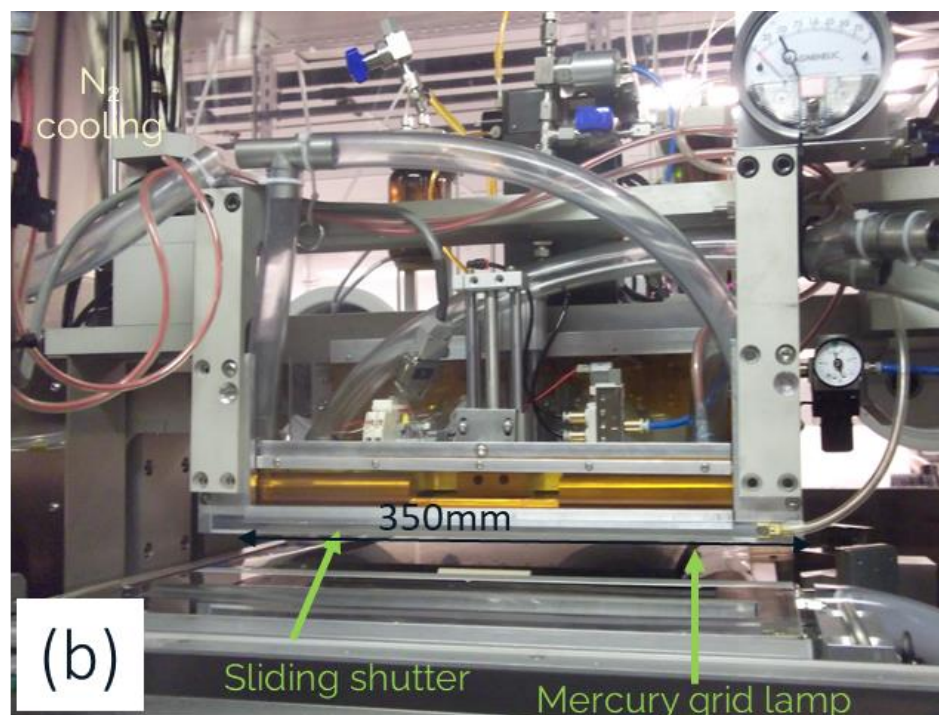
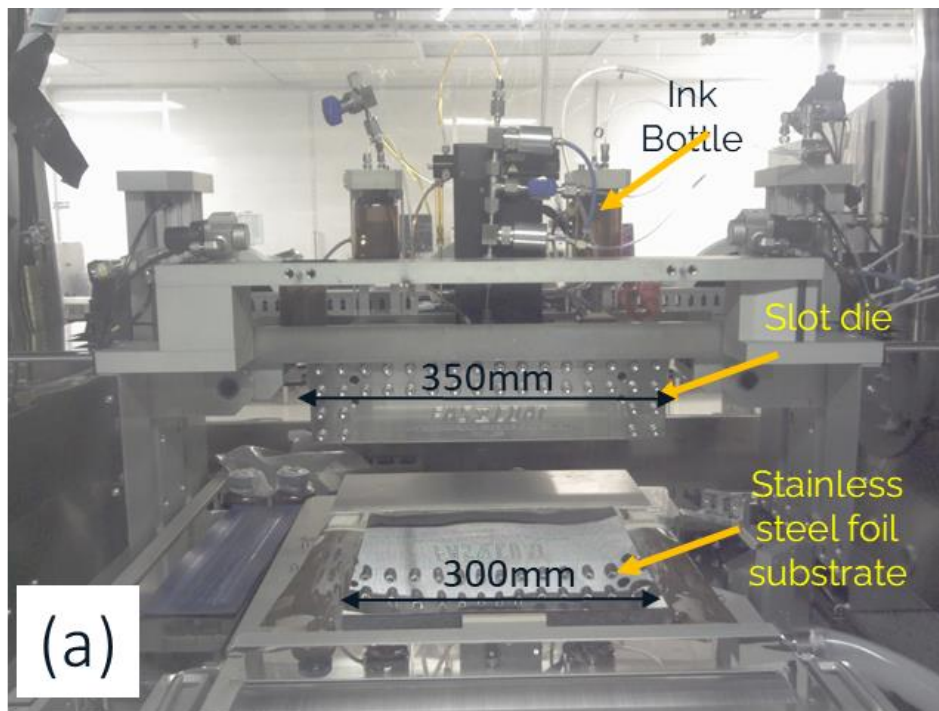


Figure 4.6: (a) Front view of the slot-die coater with the die head and the stainless-steel substrate, (b) back view of the slot-die coater with the lamp house, which was in tandem behind the slot die head.

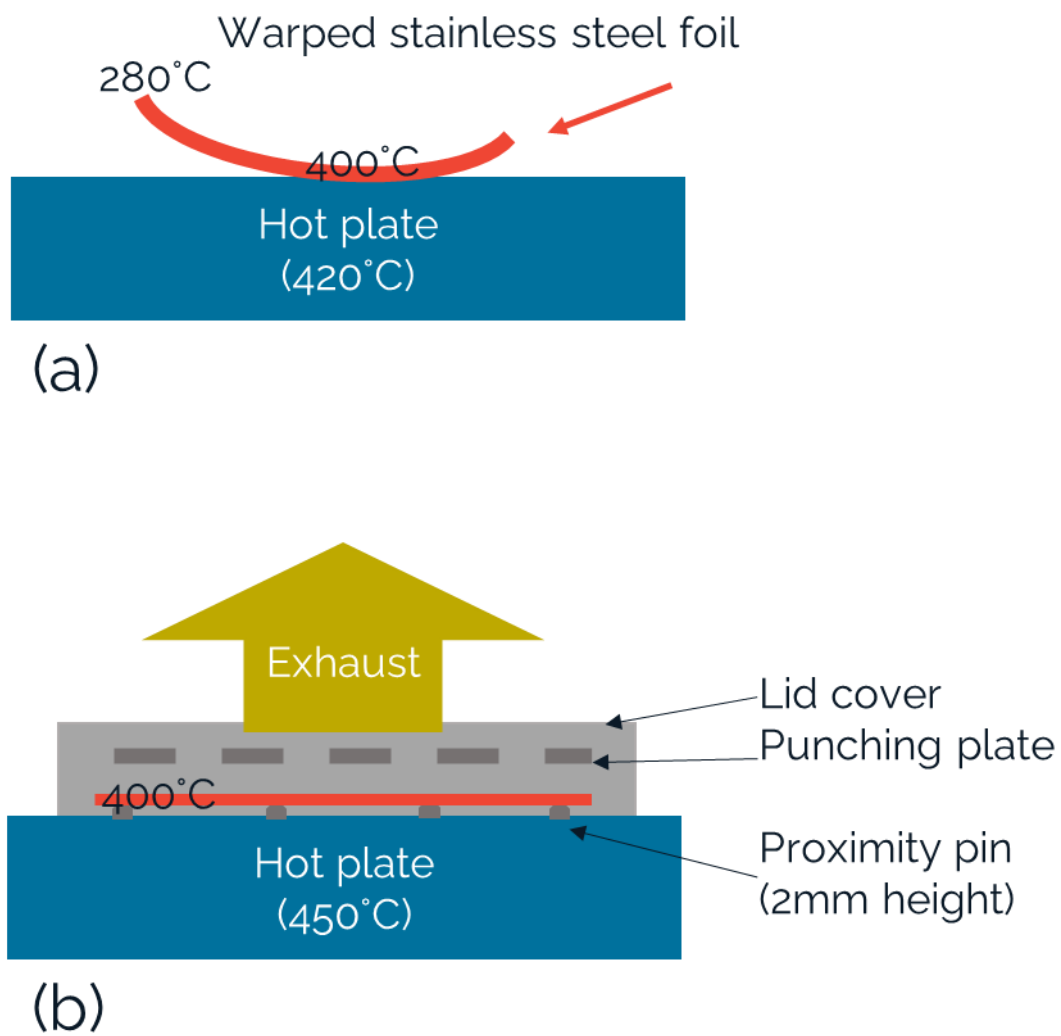


Figure 4.7: (a) Stainless-steel foil warped on a standard hotplate heated around 400°C , (b) flat stainless-steel foil on the newly developed hot plate with proximity pin, lid on exhaust

2.3. Polysilicon film formation

Mirror-polished 300 mm², 100 μm thick stainless-steel foils were fully encapsulated by a 1-μm thick engineered proprietary dielectric oxide film. Silicon ink was then dispensed on a 290 mm² area of the foil, which was cleaned by oxidation to degrease and light acid to ensure low defectivity and to provide appropriate adhesion and wettability. Because CPS evaporates at the boiling point of 194.3 °C, and poly-CPS migrates under temperature, the CPS and poly-CPS compounds were UV-treated prior to hard baking to increase their molecular weight. By increasing their molecular weight, the wet films stabilized into heat-resistant soft polymers. As Gerwig et al. demonstrated, UV irradiation cleaves Si-Si bonds generating -Si radicals and radical reactions, allowing for the generation of higher molecular weight silane polymers [20].

All exhaust from the coated surface was released simultaneously by UV irradiation. The UV wavelength was 254 nm. Its intensity at the surface of the substrate was controlled between 50–60 mW/cm². The total UV dose was controlled by the scan speed of the dispensed ink and the UV rig. The soft polymer film was then baked for 5 min on the hotplate at 400 °C. The resulting amorphous silicon film was removed from the glove box. Forty-nine equally spaced points across the 290 mm² coated area were measured for film thickness by ellipsometry, reflectometry (Tevet, Nanometric), and cross-section SEM. Then the film was subjected to a dehydrogenation bake in a furnace in ambient nitrogen for 15 hours to avoid bubbling during laser crystallization. The duration of 15 hours met the overnight manufacturing flow. The hard-cured film was analyzed using secondary ion mass spectroscopy (SIMS). The laser crystallization process was performed using a solid-state green laser. The optic specifications were wavelength: 532 nm, line width/length : 6μm x50mm, beam uniformity <10%, energy density of 1.1 J/cm², pulse duration: 500ns. The results of the dehydrogenation bakes and laser crystallization were then examined using an

optical microscope and a scanning electron microscope (SEM) to determine the best conditions for optimizing the crystalline quality.

3. Results and discussion

3.1. UV dose optimization

The optimized dispensing conditions of the wet film covering a 290 mm² area were as follows: die-slit gap = 100 μm ; dispensing rate = 120 $\mu\text{l/sec}$; coating gap = 75 μm ; and scan speed = 30 mm/sec.

Because wet films of silicon ink that was not irradiated with a sufficient UV dose beaded up from the substrate surface, they could not form a continuous film. In addition, wet films that were over UV irradiated ($> 100 \text{ mJ/cm}^2$) resulted in a hazed structure and did not form a continuous film. The latter case suggested that because the dose was excessive, the polymer in the wet film coagulated as a particulate from the solvent.

The optimum UV dosage for stabilizing the wet film of CPS ink (4 wt%) was above 70 mJ/cm^2 . The wet film of poly-CPS ink ($M_n = 1,000 \text{ g/mol}$, 4 wt%) was above 35 mJ/cm^2 . As expected, the poly-CPS film required less UV irradiation because of its higher initial molecular weight and lower volatility. With less UV, less exhaust was deposited on the quartz window of the lamp house, which, over time would otherwise decrease the UV's intensity. The maintenance of equipment in a glove box requires expensive labor and downtime. Therefore, to reduce maintenance and improve manufacturing, the poly-CPS ink was chosen for volume production.

3.2. Marangoni effect control

In the newly developed hotplate with proximity pins and lids, the variation in the substrate temperature was less than +/- 5 °C at approximately 400 °C. The temperature of the substrate on the hot plate without the proximity pins varied between 280 °C and 410 °C. After five min of hard baking on the hotplate, the hydrogen content measured by the SIMS of the slot-die coated film was equivalent to the hydrogen content of film deposited with PECVD at 350 °C, as shown in Table 2. It was also shown to contain minimal quantities of carbon, oxygen, and other impurities that directly degrade the electrical parameters of fabricated TFTs.

Figure 4.8(a) shows film thickness variations caused by the Marangoni effect. Originally, the default sequence of the coating machine separated the foil from the granite chuck immediately after coating and UV irradiation. This was in preparation for the next step in the manufacturing flow, and it was performed with pins that pushed the substrate up and off the granite chuck (Fig. 4.8(b)). However, the still wet film on the stainless steel substrate then demonstrated Marangoni flow, causing undesired film thickness variations across the foil. The Marangoni number (Mg) is a dimensionless number that compares the rate of transport caused by Marangoni flow with the rate of transport of diffusion ^[21]:

$$Mg = \frac{\Delta\sigma}{\Delta T} * \frac{1}{\eta\alpha} * L * \Delta T$$

where

σ : surface tension [N/m]

L : characteristic length [m]

α : thermal diffusivity [m²/s]

η : dynamic viscosity [kg/(s·m)]

ΔT : temperature difference [K]

Holding everything else constant, if ΔT is large, then Mg is large, which means that the variability of temperature across a substrate will cause a Marangoni flow.

Because the heat capacity of 100 μm thin foil was low, it picked up variations in air flow from the exhaust, which caused variations in temperature across the substrate, leading to a Marangoni flow, which then caused thickness variations across the substrate. The solution, therefore, was to change the manufacturing flow so that the substrate foil was not immediately removed from the granite chuck after coating and irradiation. Figure 4.8(c) shows that when the foil substrate was kept on the granite chuck, the uniformity of the film thickness improved. The temperature variation in the substrate was reduced, and the resulting Marangoni flow decreased, as shown in Fig. 4.8(d). It was theoretically assumed that before changing the process flow, ΔT was the difference in temperatures in the wet film, which was due to heat evaporation caused by varying airflow differences above the substrate, likely due to the exhaust pulled by the sirocco fan. Where the air flowed faster, the wet film below cooled more rapidly, leading to differences that caused a Marangoni flow. When the manufacturing flow was changed so that the substrate foil was not immediately separated from the chuck by the lift pins, the temperature variations in the substrate due to airflow were overwhelmed by the large heat capacity of the chuck itself, which kept ΔT small enough to prevent a Marangoni flow.

The targeted film thickness of the amorphous silicon was 85 nm. The total variation in thickness was initially approximately 7% across the sheet, as shown in Fig. 4.9(a), which became less than 5% after the Marangoni effect was suppressed, as shown in Fig. 4.9(b).

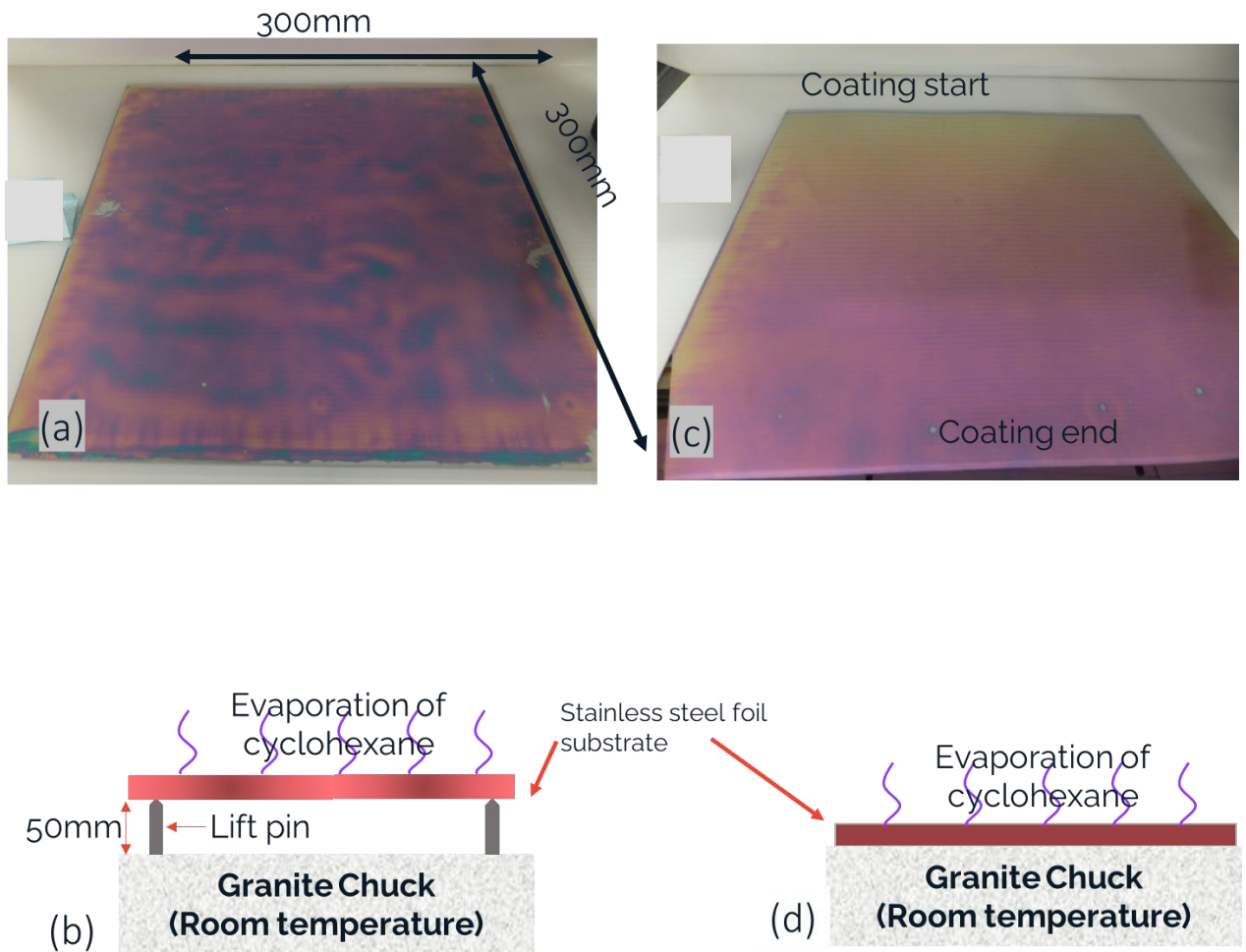


Figure 4.8: (a) Thickness variability of coated poly-CPS film, (b) model of evaporation of cyclohexane on the substrate on the lift-pins, (c) poly-CPS film with improved thickness uniformity, and (d) model of evaporation of cyclohexane on the substrate on the granite chuck

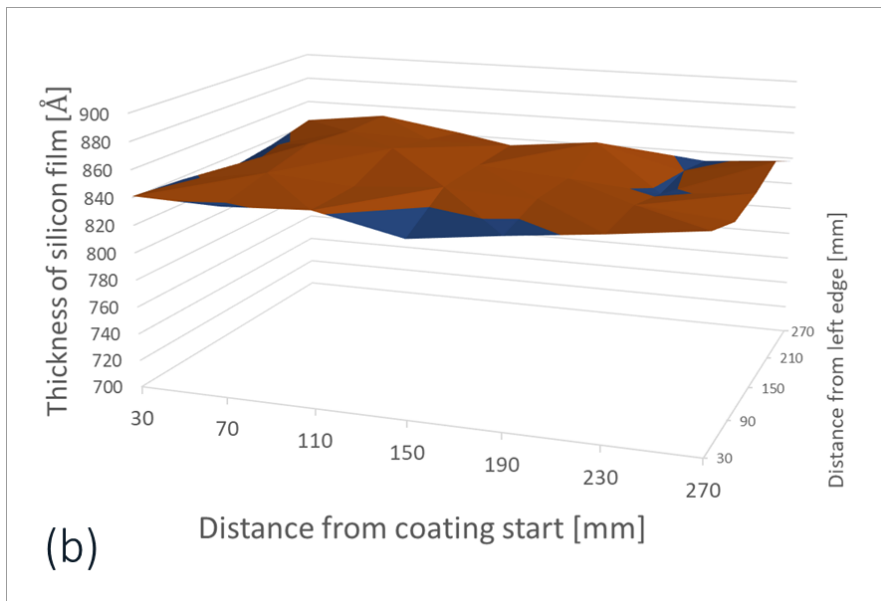
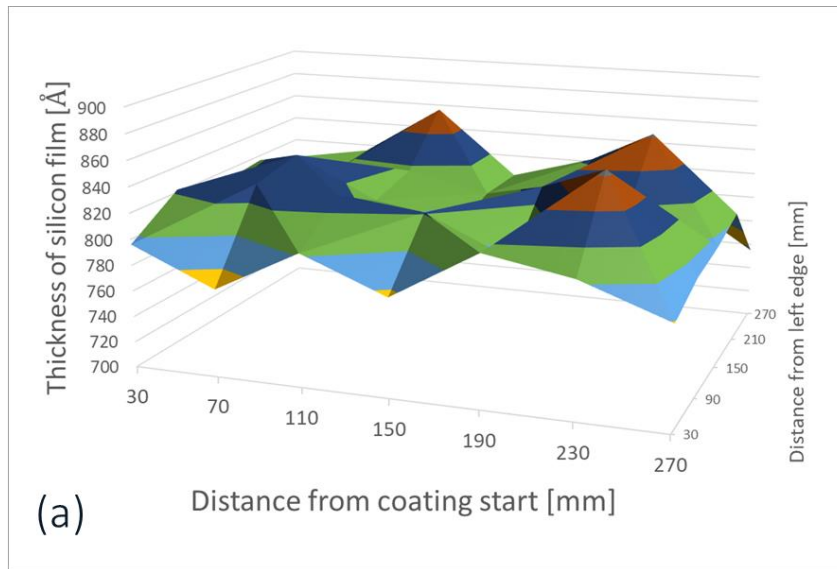


Figure 4.9: Variations in film thickness across a 300 mm sheet (a) dried on the lift-pins with a large Marangoni effect and (b) dried on the granite chuck

3.3. Particle control

In UV irradiation, fumes emanating from the coated surface were observed. Some were deposited as a brown film on the quartz window of the lamp house. In addition, some particulate matter was observed by an optical microscope on the surface of the silicon film on the substrate. Figure 4.10 (a) shows the spectrum of Auger electron spectroscopy (AES) of the particles. The composition of the particles was mainly silicon and a small amount of oxygen. This was judged to be part of the fumes that had been emitted as particles. As the result the exhaust prevented particles from depositing onto the coated surface. Images taken by a differential interference contrast microscope after hard baking and particle counts generated by image analysis are shown in Fig. 4.10(b) and (c), revealing the surface without and with exhaust during UV irradiation. This proved that exhausting was effective in preventing particles from falling onto the silicon film surface.

To obtain silicon film with a thickness of 80–90 nm on an area of 290 mm² after hard baking, the slot die process required 1 ml of 4 wt% ink that contained 0.048 mg/cm² of neat poly-CPS. Spin coating, which was performed in previous work, on a 100 mm diameter silicon wafer required 1 ml of 15 wt% ink, which contained 1.9 mg/cm². For blank film coating, the slot die process required 40 times less neat poly-CPS than the spin coating required per cm².

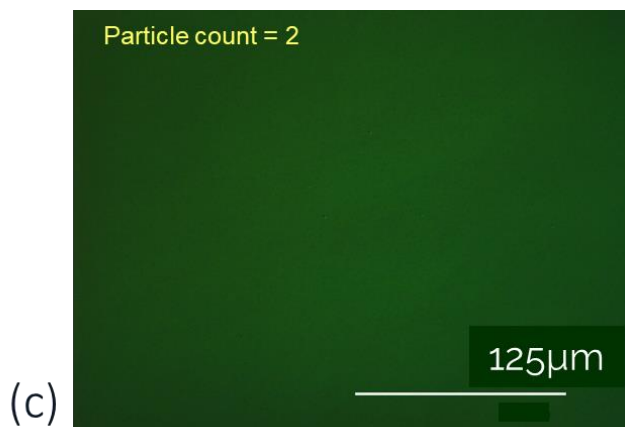
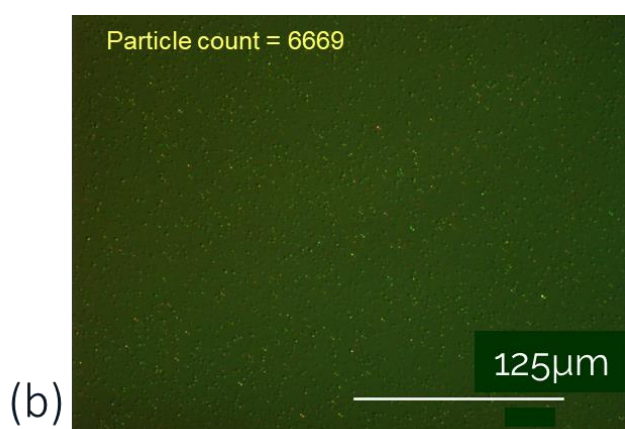
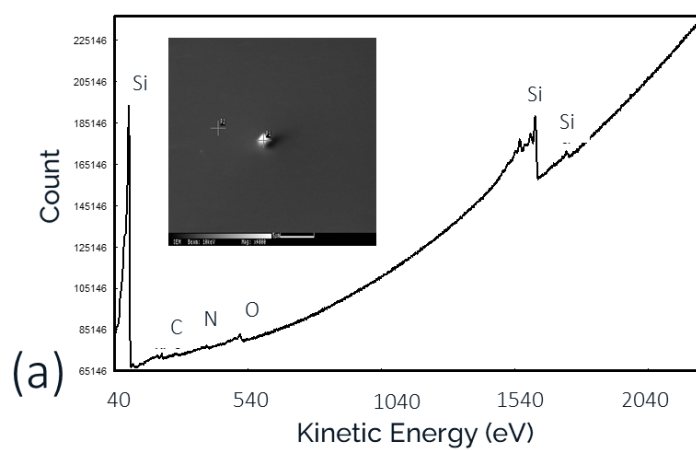


Figure 4.10: (a) AES spectrum of the particle, microscope images, and particle counts evaluated with image analysis after hard bake the surface of coated poly-CPS ink, (b) without and (c) with exhaust during UV irradiation

3.4. Laser crystallization

3.4.1. Dehydrogenation bake

In Chapter 1, in a previous study on spun films of CPS on silicon wafers, excimer laser irradiation resulted in bubbles caused by high hydrogen content in the film. In that study, a dehydrogenation bake at 550 °C for 15 hours in nitrogen gas flow prevented the film from forming bubbles. Table 4.1 shows that the hydrogen content of the amorphous silicon film in the previous work decreased to less than 1 atm% after dehydrogenation baking at 550 °C for 15 hours [22]. The hydrogen content of spun film, which was studied in a dehydrogenation bake using rapid thermal anneal (RTA) at 700 °C for 2 min in nitrogen gas, also decreased less than 1 atom%. A SIMS analysis of various dehydrogenation bakes was investigated with slot-die coated film and PECVD film. Because stainless steel foil substrate warps, heating equipment, such as RTA, cannot be used.

Table 4.1. SIMS analysis of silicon film post dehydrogenation bake

Deposition method	Hard bake	Hydrogenation bake	C [atm%]	H [atm%]	O [atm%]	N [ppm]
Spin coat	Muffle oven 400 °C 20 min	NA	0.031	8.00	0.020	1.0
		Muffle oven 550 °C 15hr	0.010	0.56	0.020	7.0
Slot-die	Hot plate 450 °C 5 min	NA	0.035	22.64	0.161	63.1
		Furnace 650 °C 30min in N2	0.022	0.37	0.132	88.3
		Furnace 550 °C 15hr in N2	0.021	0.26	0.157	81.4
PECVD at 350°C	NA	NA	0.001	21.90	0.020	13.4
		Furnace 550 °C 15hr in N2	0.004	0.21	0.017	22.9

Therefore, a furnace was used for the dehydrogenation bakes. The hydrogen content of both the slot-die coated film and the PECVD film on the stainless steel foil was decreased to less than 1 atm% at 550 °C for 15 hours. In the next step, when the sheet process was moved to the roll-to-roll process, the condition of 700 °C for 2 min was applicable because stainless steel foil can be heated without warping using the roll-to-roll process with tension.

3.4.2. *Laser condition vs. defect*

Figure 4.11 shows a comparison of the laser crystallization of the 75 nm thick a-Si film that was deposited by PECVD in the slot die-coated poly-CPS silicon ink film process, which included the dehydrogenation bake and laser dose. Films subjected to a 15 hour bake at 550 °C did not show any bubbles, as expected. The a-Si film deposited by PECVD produced elongated crystalline growth within an hour of baking and a 1300 mJ/cm² laser dosage. The slot-die coated process of poly-CPS film produced elongated crystalline growth in a 15 hour bake at 550 °C with a 1300 mJ/cm² dosage. Figures 4.12(a) and (b) show top views and cross-section images by a scanning electron microscope (SEM) of laser irradiated slot-die coated poly-CPS film with a dosage less than 1100 mJ/cm². The images show that crystalline growth stopped horizontally and formed bumps that were 50 nm high in marginal areas. Figures 4.12(c) and (d) show the film irradiated with the optimum of 1300 mJ/cm². Under these conditions, the crystals grew laterally and were smooth with the grain. Figure 4.13(a) shows the top view of the SEM image with the Secco etch. Elongated crystals were clearly observed. With optimal dehydrogenation bake and laser irradiation, excellent crystallization uniformity was observed across the 300 mm substrate. Figure 4.13(b) shows a high-resolution transmission electron microscopy (TEM) image that reveals a clear grain lattice.

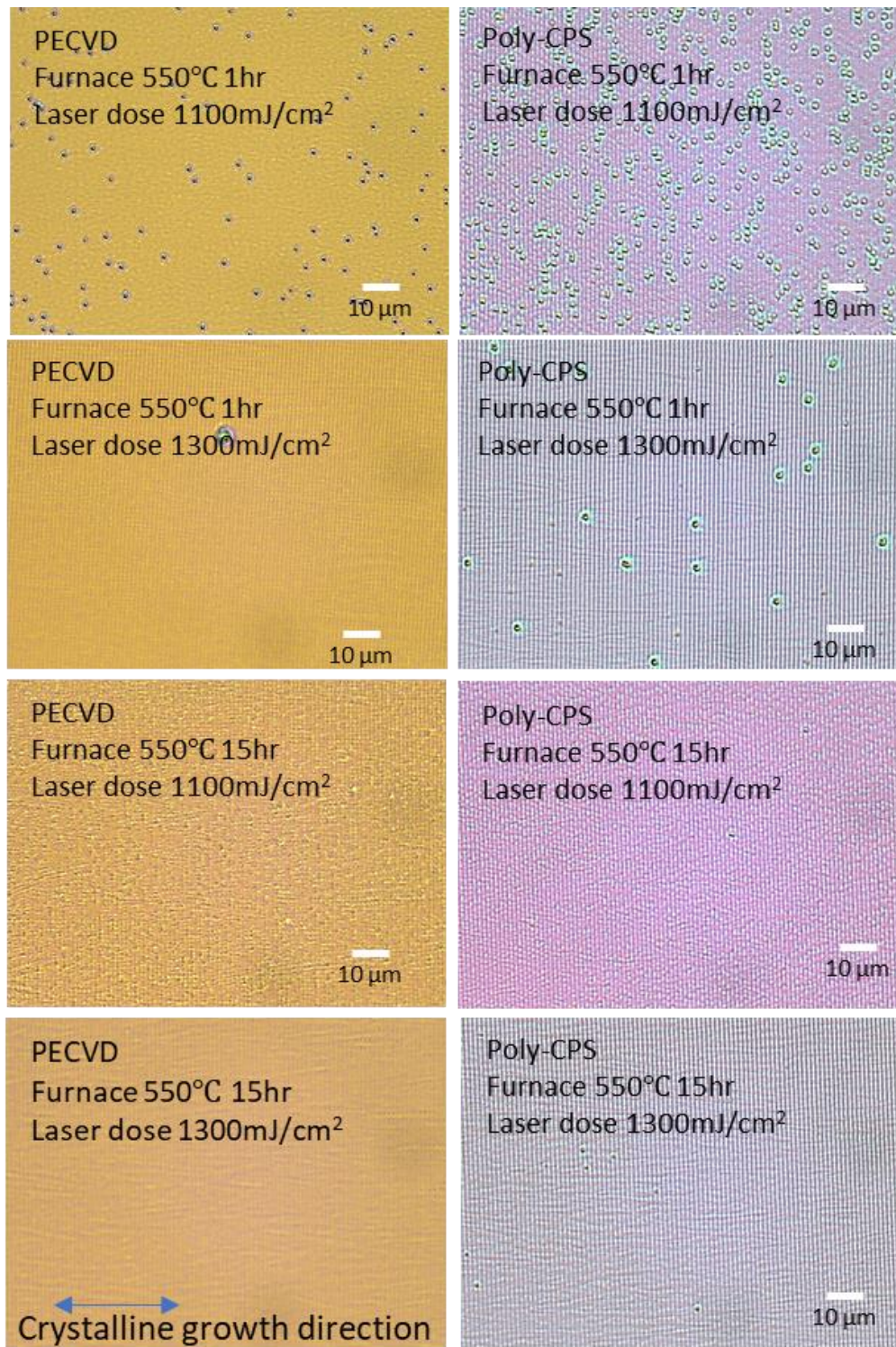


Figure 4.11: Optical microscope image (x2500) of coated poly-CPS silicon ink film and PECVD film after solid-state laser crystallization under various dehydrogenation bake conditions

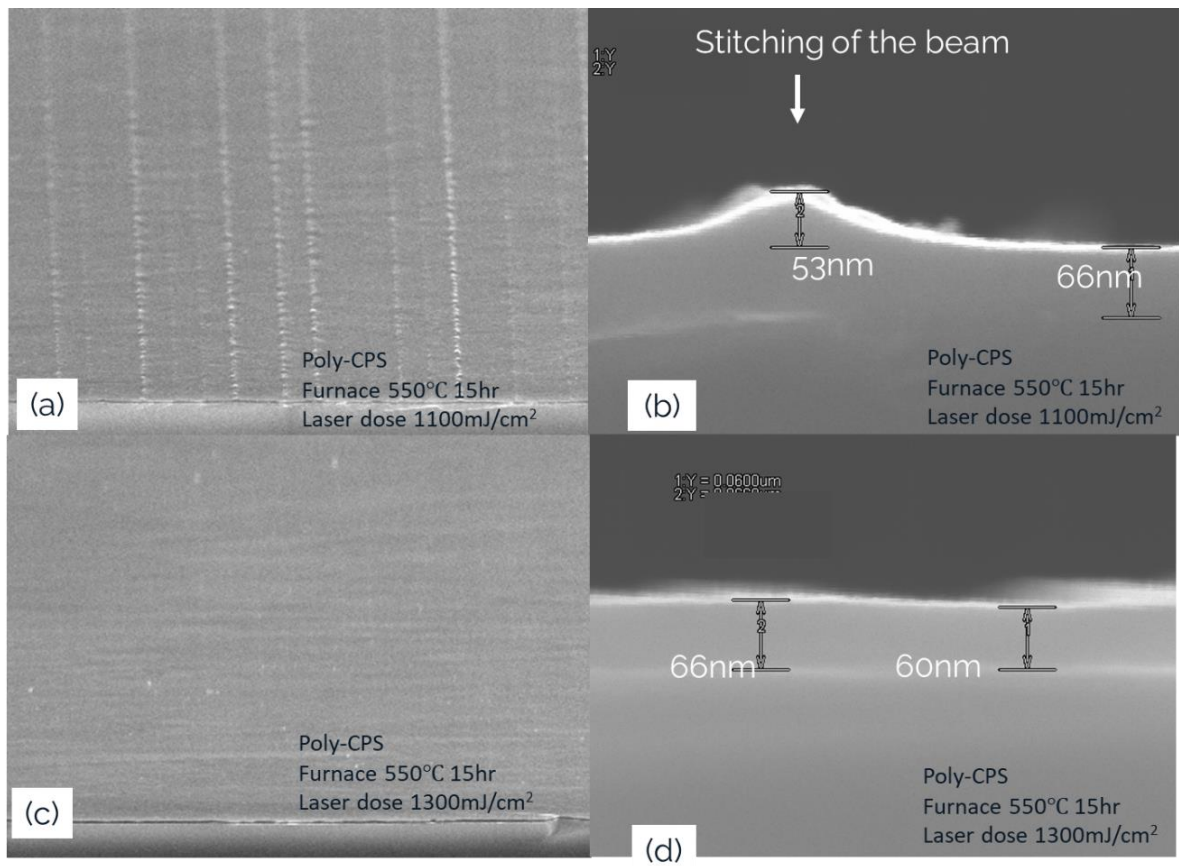


Figure 4.12: (a), (b) Top view and cross section view SEM image of laser annealed poly-CPS silicon ink film with 1100mJ/cm², (c), (d) Top view and cross section view SEM image of laser annealed poly-CPS silicon ink film with 1,300 mJ/cm²

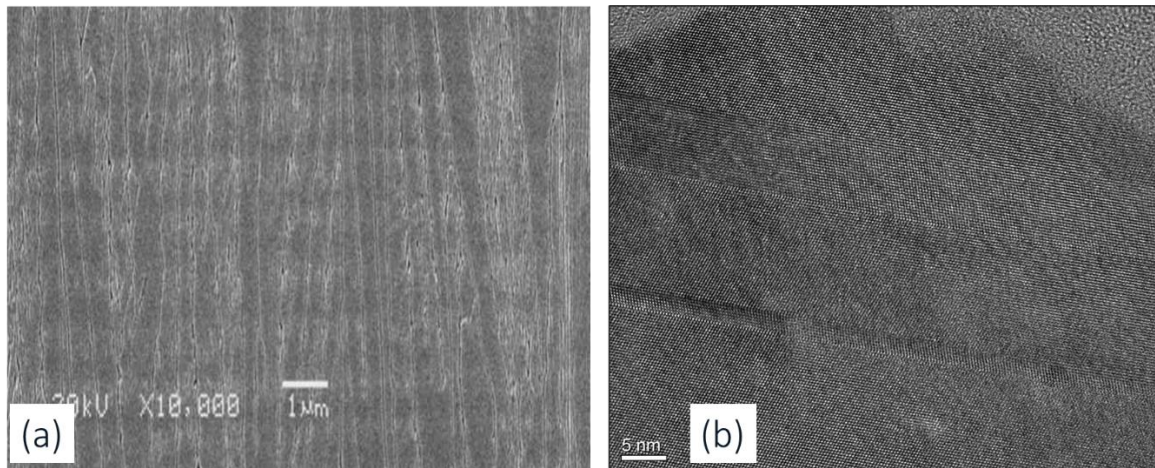


Figure 4.13: (a) SEM image of laser annealed poly-CPS film with Secco etch, (b) high resolution cross section TEM of the crystallized silicon layer

4. Conclusion

To build a hybrid flow of conventional lithography and printing, slot-die coating of silicon ink and the formation of polysilicon film were studied with lithography to form channels that replaced a large part of inkjet-only printing, which was found to be too immature for industrial purposes.

A slot-die coater integrated with the UV lamp house in the glove box was designed and tested. A hotplate with a proximity pin and lid was also designed and tested for uniform and fast hard baking. The formulation of novel in-house inks for slot-die coating was investigated. A monomer CPS ink and a poly-CPS ink were formulated as precursors of silicon film. These were UV-treated to increase their molecular weight and stabilize them before hard baking, and they were laser crystallized to form an amorphous silicon film. The inks were slot-die coated on a 300 mm² 100- μ m thick stainless steel foil substrate that was compatible with the high-temperature ink processing required. The coating parameter was optimized for target thickness, and the Marangoni flow was controlled for uniform thickness. As a result, approximately 60 nm (+/- 5%) thick amorphous films were obtained consistently in the manufacturing environment.

Finally, dihydrogen baking and laser crystallization were studied and optimized to form elongated crystalline without defects. The result was the production of nearly equal PECVD quality in a flexible silicon-coated substrate that was ready for next-step doping, layering, and channeling.

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Chapter 5

Screen Printable N⁺ and P⁺ Dopant Inks

1. Introduction

1.1. Research objective

In this chapter, the development of the P⁺ and N⁺ dopant ink formulations used in screen printing and the characterization and doping process of polysilicon TFTs are described. In Chapter 1, the previous development of entirely inkjet printed TFTs and spin-on dopants (Honeywell B-30, P-8545) were used as the basis for the dopant ink ^[1]. In this process, multiple issues were identified. In addition to the inadequacy of the equipment, there were problems with the ink. In production, after thermal annealing for activation, the ink left a glassy dopant residue that was difficult to remove without damaging the TFTs. The boron ink was highly moisture-sensitive, and it lost doping capability after it was exposed to air. Therefore, to develop screen-printable dopant inks, a different approach needs to be taken.

The concept of screen-printable dopants was introduced in the photovoltaic (PV) industry by Hilali et al. ^[2] and Edward et al. ^[3] in the early 2000s. In the last decade, multiple screen printable dopant processes for the PV industry have been developed ^[4,5]. Many screen printable inks (often called “paste” in the PV industry) were formulated with inorganic particles, such as silicon or alumina particles ^[6, 7], or a sol-gel base ^[8, 9] that required harsh chemicals to remove the residual layer after thermal activation. Dipping TFTs in harsh chemicals, such as buffered oxide etch (BOE), long enough to remove the residual layer remove or damage the thin polysilicon layer and gate oxide. Therefore, in TFT fabrication, a different approach was also needed.

Our goal was to develop screen-printable dopant ink formulations and processes that offered high print fidelity, a manageable queue time (q-time), allowing for fabrication without degrading the dopant inks, and an inoffensive residue removal process. Such inks would ultimately enable scaling to ultra-high-volume roll-to-roll production using high-speed, low-cost techniques, such as slot die coating or rotary printing.

Our dopant inks were created for screen printing by adding boron or phosphorous compounds to an ink vehicle formulated by a solution of thermoplastic polymers. Multiple thermoplastic polymers, such as polymethyl methacrylate, polystyrene, or poly-isobutyl-methacrylate (IBMA), are known to act as binders of ceramic or metal paste. They burn off cleanly at 300–400 °C during sintering ^[10]. These binders are also used to control porosity in ceramics ^[11]. A thermoplastic polymer is used because it is inherently hydrophobic. Therefore, they protect the boron dopant at the silicon interface from ambient humidity. Otherwise, the boron compound chemically reacts with water to become boric acid and evaporates at 350 °C, which is below the activation temperature ^[12, 13]. This protection also provided the generous requisite queue time (q-time) between print and thermal activation without the dopant degradation required in manufacturing. After activation following the polymer burn-off, a porous dopant layer was expected to remain, and its porosity was expected to make the residue easy to remove. Instead, a carbon residue was produced, which preserved the boron dopant at the interface. The thin carbon residue was easily removed. Finally, to maximize print fidelity, the combination of polymer and solvent had to be optimized for viscosity and screen drying time.

1.2. Screen printing general theory

Screen printing is a printing technique in which a mesh is used to transfer ink onto a substrate, except in areas impermeable to the ink by a blocking stencil. Figure 5.1 shows the sequence used in screen printing. A blade or squeegee is moved across the screen to fill the open mesh apertures with ink, and a reverse stroke causes the screen to touch the substrate momentarily along a line of contact. This causes the ink to wet the substrate and to be pulled out of the mesh apertures, as the screen springs back after the blade has passed. Screen printing has the flexibility to print on a variety of materials in shape, topology, and roughness. In addition, ink components can be designed and selected relatively freely. Recent technological advances have made it possible to print fine wiring of only 10 μm using a printing method that meets the needs of the production of electronic components. Different types of mesh size, attack angle, and hardness of the squeegee will determine the thickness and print resolution of the material. When a higher mesh gauge, higher attack angle, and harder squeegee are applied, the deposited ink is thinner and produces a higher resolution.

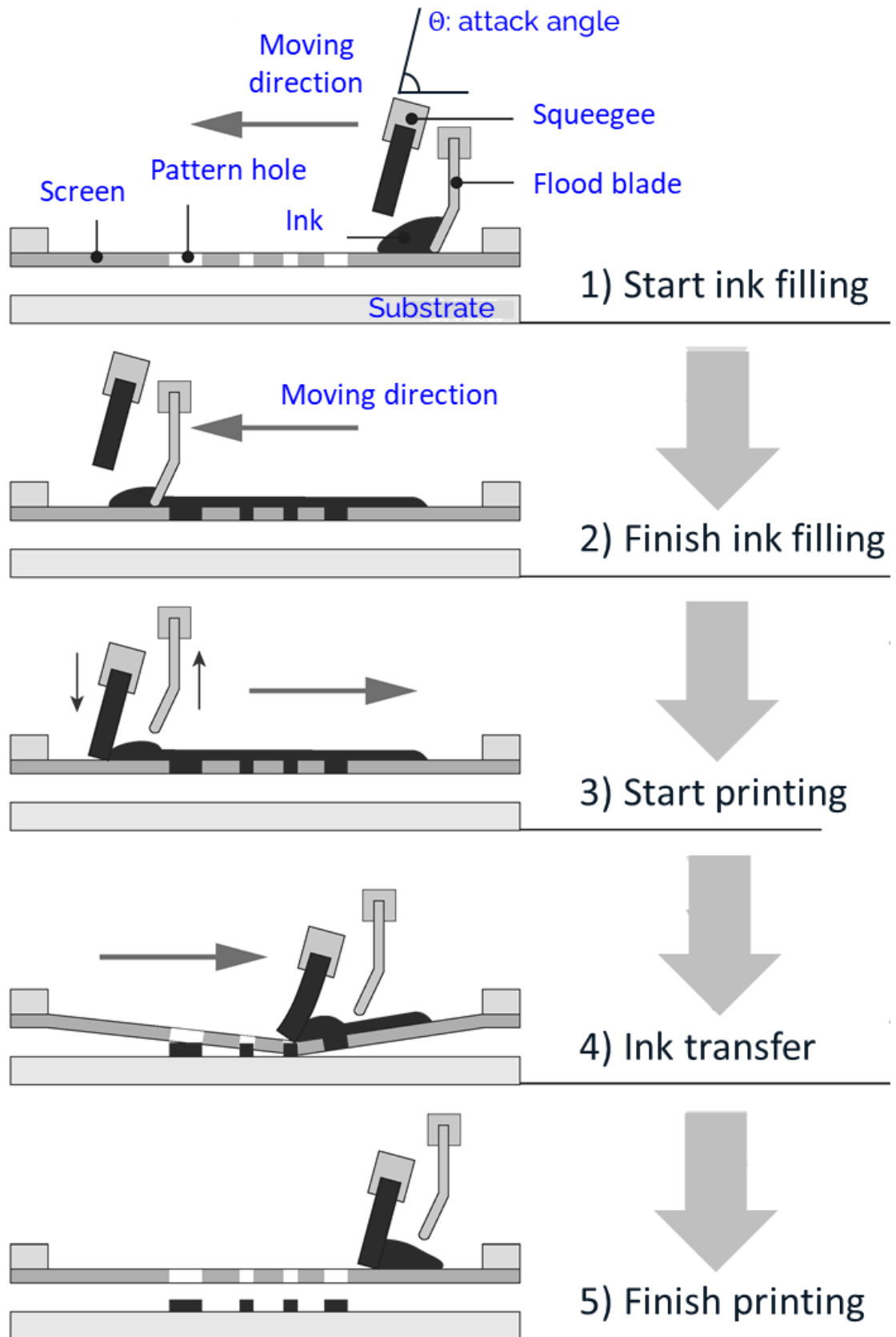


Figure 5.1: Diagram of screen printing

This process was traditionally called silkscreen printing because silk was used. Currently, a variety of synthetic threads are used in the screen-printing process. The most popular mesh in general use is made of polyester. The electrical industry typically uses mesh materials made of nylon, polyester, and stainless steel.

Figure 5.2(a) shows a screen mask. The screen size needs to be three times larger than the printing area to avoid distortion of the print image. Figure 5.2 (b) shows the details of the photo-imaged emulsion on stainless-steel mesh. The mesh material was assembled on an aluminum frame under tension, and then the emulsion was coated and imaged.

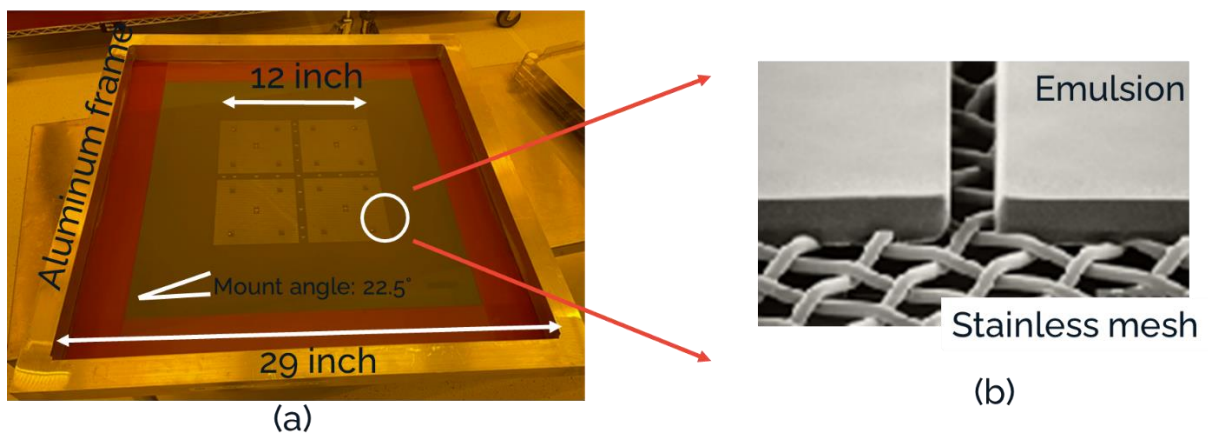


Figure 5.2: (a) Screen mask for printing 12-inch square substrate, (b) microscope image of the emulsion pattern on stainless steel mesh

2. Experiments

2.1. Ink formulation and characterization

Figure 5.3 shows the ingredients used to formulate the P+ and N+ dopant inks.

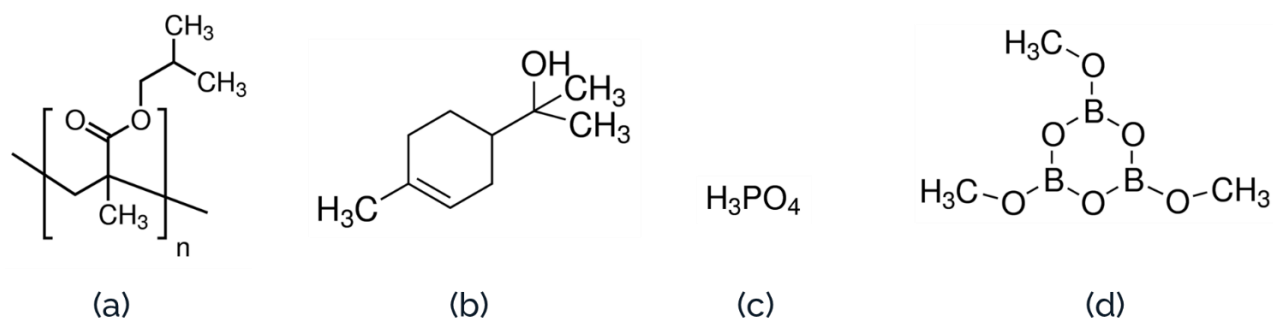


Figure 5.3: Constitutional formula of (a) Poly-IBMA, (b) α -terpineol, (c) phosphoric acid, and (d) trimethoxyboroxine

Poly-IBMA (Sigma Aldrich) was dissolved in α -terpineol (90% Sigma Aldrich). Trace metal was then removed from the solution using a proprietary process. The viscosity of the resulting solution was measured using a Brookfield RVDV-U-CP rheometer with a CP51 cone spindle at 0.6 rpm at 21 °C. Mass loading was measured via thermal gravimetric analysis (TGA) under ambient nitrogen. The trace metal impurity of the solution before and after purification was evaluated using inductively coupled plasma mass spectrometry (ICPMS).

Phosphoric acid (85 w% in H_2O , > 99.999% trace metals basis, Sigma Aldrich) was then added as the N+ dopant source, and additional α -terpineol was added to control viscosity. This solution was stirred to formulate the N+ dopant ink. The P+ dopant ink was formulated by adding trimethoxyboroxine (TMB, 95%, Sigma Aldrich) as the P+ dopant source. Additional α -terpineol was again added to control viscosity. Proprietary spin-on-glass (SOG) was added to the P+ ink to control pitting on the field oxide surface. The TGA and viscosity

at various spindle speeds were measured. The viscosity of the inks was adjusted to 60,000 cps at 0.6 rotations per minute (rpm).

2.2. Study of print condition

A DEK Genesis screen printer was used. The screen masks (DEK) were made of 29" x 29" aluminum tube frames made of 400-gauge stainless-steel mesh 48 μm thick with a wire diameter of 25 μm , mounted at an angle of 22.5°. The screen tension was 28 +/- 2.5 N/cm. To maintain the printed thickness at 5–7 μm , the emulsion thickness of the P+ ink was 13 μm , and the emulsion thickness of the N+ ink was 5 μm . The shore hardness of the polyurethane 370 mm long squeegee was 90–100, and the attack angle was 60°. Figure 5.4 shows the printing patterns of the P+ and N+ inks in a die. Across the 300 mm² sheet, the print pattern of the N+ ink was approximately 13000, 1.0 x 4 mm rectangles. The print pattern of the P+ ink was approximately 13000, 0.5 x 4 mm rectangles. To obtain optimum image quality and uniformity, both dopant inks were printed with various print gaps at different squeegee speeds. Printed patterns were observed under a microscope (Keyence), and thickness was measured using a profilometer (Tencor, P-20). The latency of the inks on the screen was evaluated. The printed inks were soft baked on a hot plate at 80 °C for 5 min under hot air flow. The hot plate was designed with the laminar flow of hot air above to produce a uniform and crisp print image.

2.3. Activation

Stainless steel foil 300 mm² was completely encapsulated by a proprietary barrier layer and a dielectric insulator to prevent diffusion of trace metals from the substrate during thermal annealing. A 70-nm thick amorphous silicon layer was deposited using either plasma-enhanced chemical vapor deposition (PECVD) or slot-die coated silicon ink, which then received a dehydrogenation bake. This was subsequently irradiated and crystallized with a solid-state laser. Figure 5.4 (b) shows a printed dopant and annealing scheme. Dopant inks were printed on the active layers and annealed in ambient nitrogen in a furnace at various temperatures. Sheet resistivity was measured using a four-point probe after the residue was removed. The surface was observed using a microscope or secondary electron microscopy (SEM). The surface residue was analyzed using X-ray photoelectron spectroscopy (XPS). Various ink compositions were printed and activated to investigate the effects of active content on sheet resistance. The comparative effects of the length of q-time between printing, soft baking, and activation annealing on sheet resistance were also evaluated. After activation annealing, the substrate was treated with O₂ plasma ashing to remove carbon residue and then dipped in diluted hydrogen fluoride acid (HF, 500:1) for 10 min to remove the remaining boron and phosphorus oxide.

A critical element of CMOS functionality was the absence of the cross-contamination of the N⁺ and P⁺ dopant inks thorough vapor transport. Sheet resistance was measured as a function of the distance from the printed line.

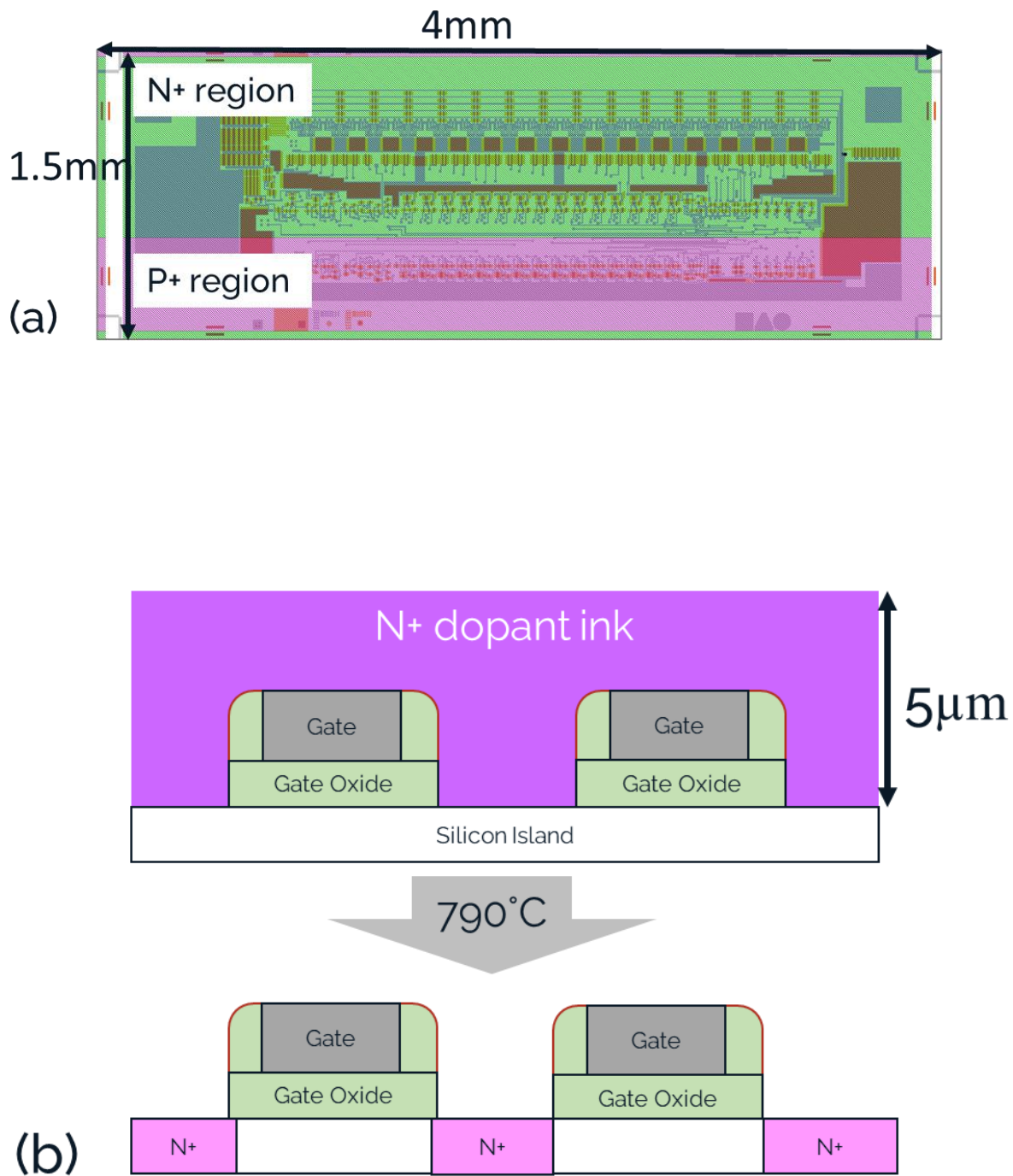


Figure 5.4: (a) N+ region and P+ region of printing dopant on an NFC circuit, (b) self-aligned doping process using screen printed dopant ink

3. Results and discussion

3.1. Ink characterization

3.1.1. Polymer vehicle purity

Table 5.1 shows the ICPMS result of the poly-IBMA solution in α -terpineol before and after purification. The levels of all trace metals in the solution were less than 20 ppb after purification, which achieved CMOS grade. The viscosity of the solution was approximately 80,000 cps. The TGAs of the poly-IBMA powder and the poly-IBMA solution after purification are shown in Fig. 5.5(a) and (b). The α -terpineol's weight was decreased at temperatures less than 190 °C, and the polymer's weight was eliminated at temperatures less than 400 °C. In both cases, all polymers and solvents were burned off, and no residue was observed. The mass loading of the purified solution was approximately 45 wt%.

Table 5.1: ICPMS measurement of trace metals before and after purification of the poly-IBMA solution

Metal	Mg	Al	Ca	Fe	Cr	Ni	K	Cu	Zn	Na	Ti
Detection limit [ppb]	0.03	0.2	0.1	0.1	0.02	0.05	0.1	0.01	0.04	0.03	0.03
Before purification [ppb]	150	110	690	<0.1	20	<0.05	100	1.2	9.8	2500	2.3
After purification [ppb]	<2	<2	12	<5	<5	<2	<5	<2	<2	20	<2

3.1.2. TGA analysis

Figure 5.5(c) shows the comparison of the TGAs of the P+ ink and the purified polymer solution. The loss of both solvent and polymer was delayed in comparison with the polymer-only solution. This delay indicated an interaction between the active ingredients and both the solvent and the polymer in the P+ ink. The P+ ink left a black residue of 1.5%. Figure 5.5(d) shows the TGA of the N+ ink. The loss of polymer was also delayed in this case, whereas the loss of solvent was not delayed. An interaction was observed between the phosphoric acid and the polymer. The N+ ink also left a black residue of only 0.5%.

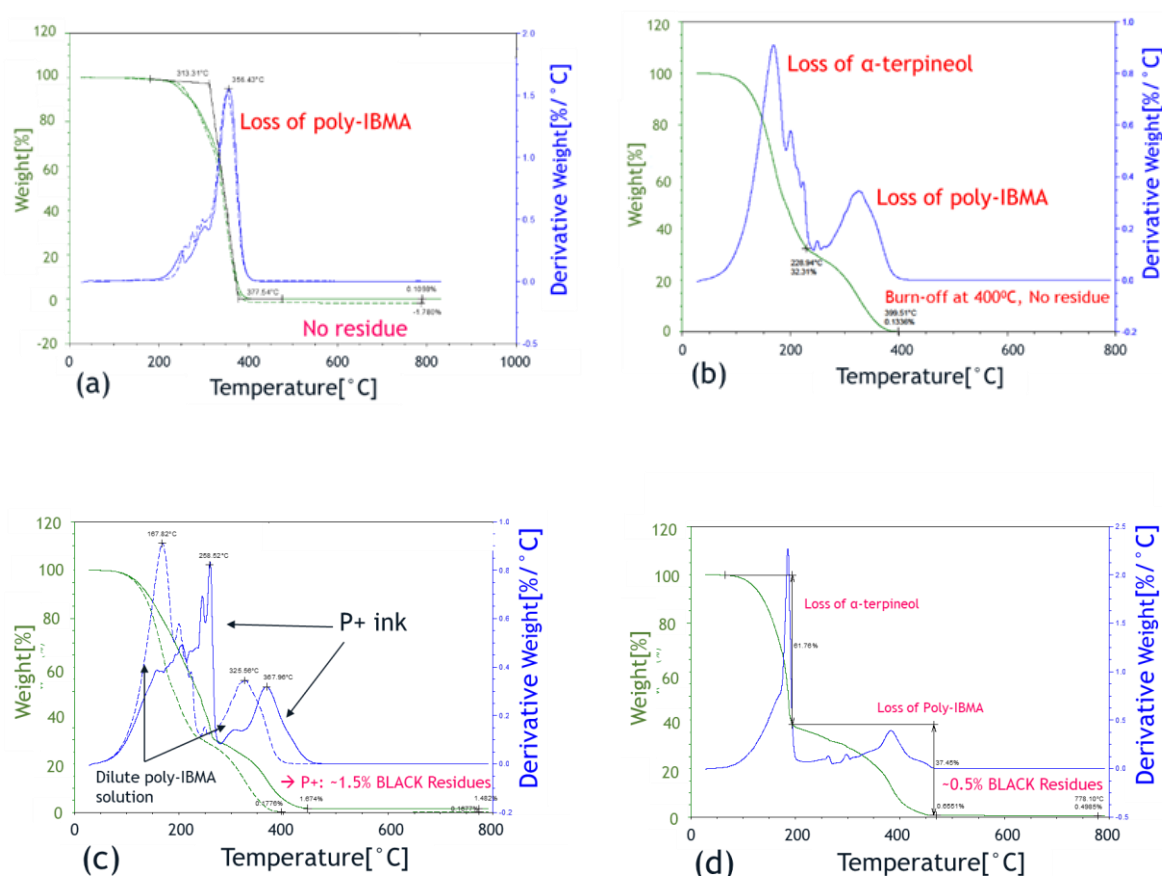


Figure 5.5: TGA of (a) the poly-IBMA and (b) the poly-IBMA solution in α -terpineol after purification, (c) comparison of the P+ ink and the poly-IBMA solution, and (d) the N+ ink

3.1.3. Viscosity

Figure 5.6 shows the viscosity of the P+ ink and the N+ ink versus the spindle speed. Both the P+ and N+ inks showed significant shear speed dependence at low speeds < 0.1 rpm, which was more obvious in the viscosity of the P+ ink. There was no obvious effect at high speeds > 0.2 rpm. The standard testing speed was 0.6 rpm. The thixotropic index (0.02 rpm/0.2 rpm) of the P+ ink and the N+ ink were 2.8 and 1.7, respectively. The P+ ink should have behaved like a thixotropic fluid, while the N+ should have behaved like a Newtonian fluid.

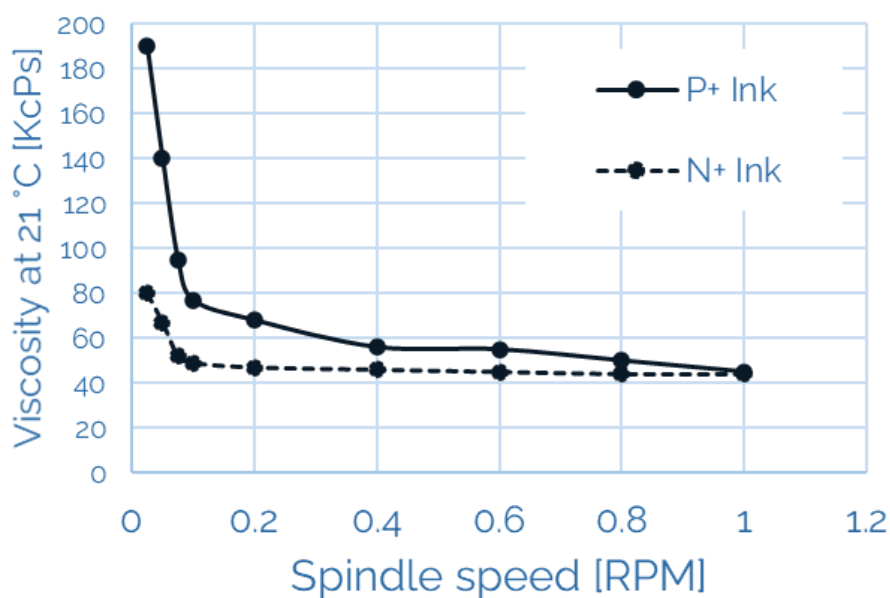


Figure 5.6: The viscosity versus the spindle speed of the P+ and N+ inks

3.2. Print characterization

3.2.1. Print gap

The P+ ink and N+ inks were printed at various print gaps and print speeds, as shown in Figure 5.7. Figure 5.8(a) shows printed pattern images of the P+ ink with 2 mm and 4 mm print gaps. The printed pattern profiles were measured using a Tencor profilometer on the left, center, and right sides. Poor snap-off was observable below 3 mm print gaps. Increased thickness, surface roughness, and loss of uniformity were associated with poor snap-off. The print gap needed to be increased to > 3.5 mm to obtain a clear printed image and a uniform thickness across the 300 mm sheet. Across the sheet, profile variability was reduced when snap-off was improved. Further increases in the print gap reduced the screen's lifetime. Figure 5.8(b) shows printed pattern images of the N+ ink with print gaps of 2 mm and 4.5 mm. With a narrow print gap < 3 mm, the ink was smeared into spaces and bridged between patterns. A print gap wider than 4.5 mm caused the printed thickness to become even across the sheet. At the edges, printed patterns showed fringes caused by ink smearing along the mesh wire, which was due to the Newtonian characteristic of the N+ ink.

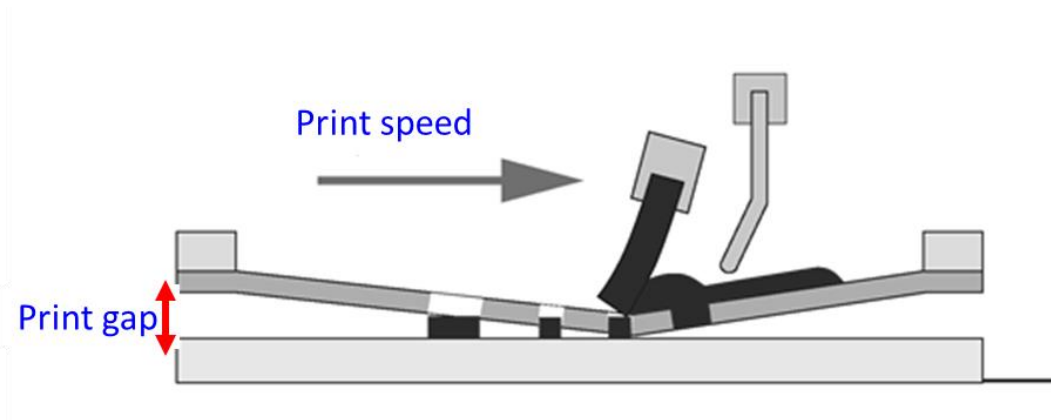


Figure 5.7: Print gap in screen printing

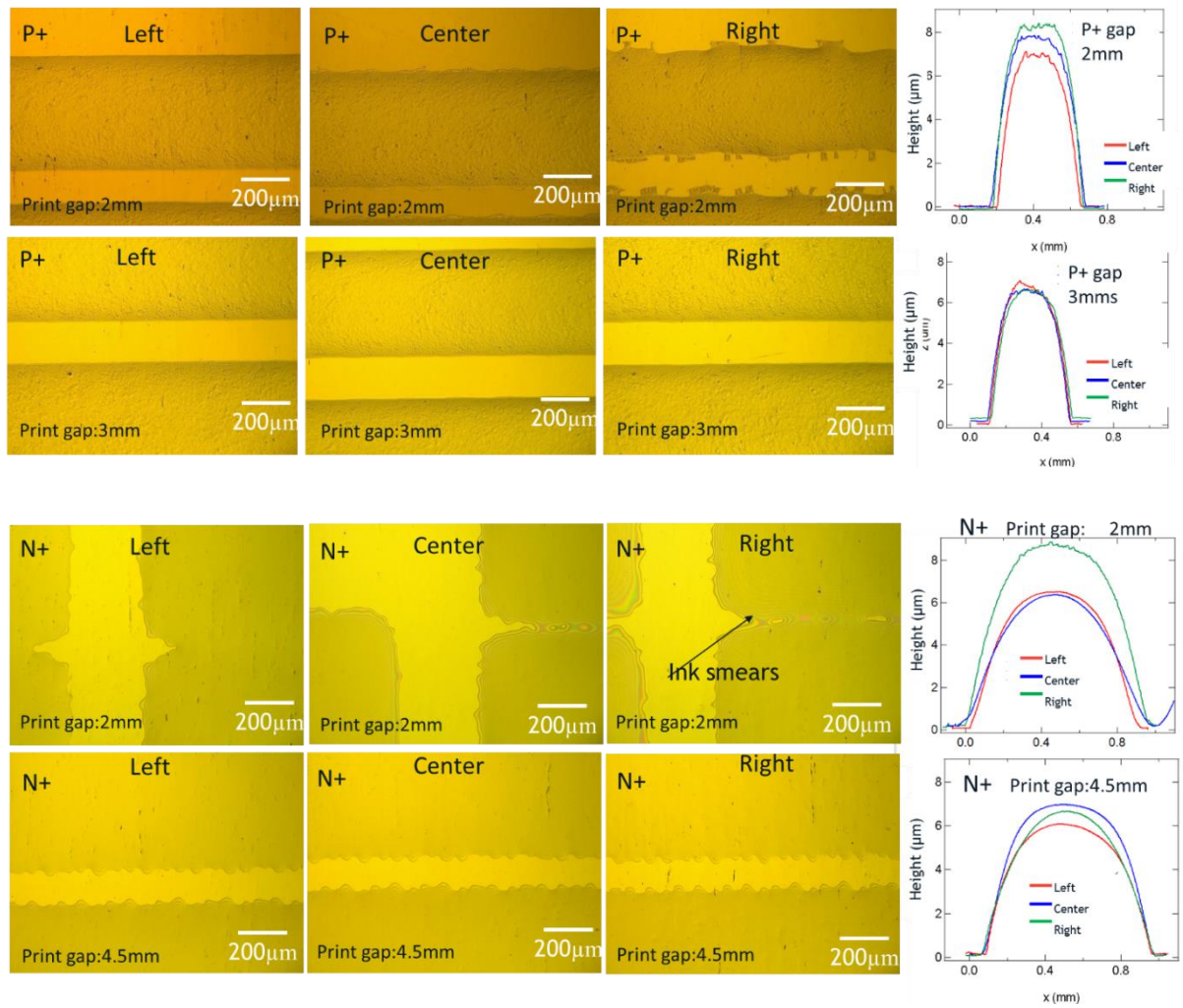


Figure 5.8: Optical microscope image (x250) and cross-section profile of (a) the printed P+ and (b) N+ inks at various print gaps (P+: 2 mm and 3 mm, N+: 2 mm and 4.5 mm). Left-, center-, and right-side positions. Print speed: 20 mm/s, Pressure 9 kg.

3.2.2. Print speed

Figure 5.9 shows printed pattern images of both P+ and N+ inks at various squeegee speeds. Fast squeegee speeds caused poor snap-off and poor uniformity across the sheet. Narrower print gaps or faster print speeds increased the roughness of the surface, which, however, could be disregarded because the dopant was burned off during annealing.

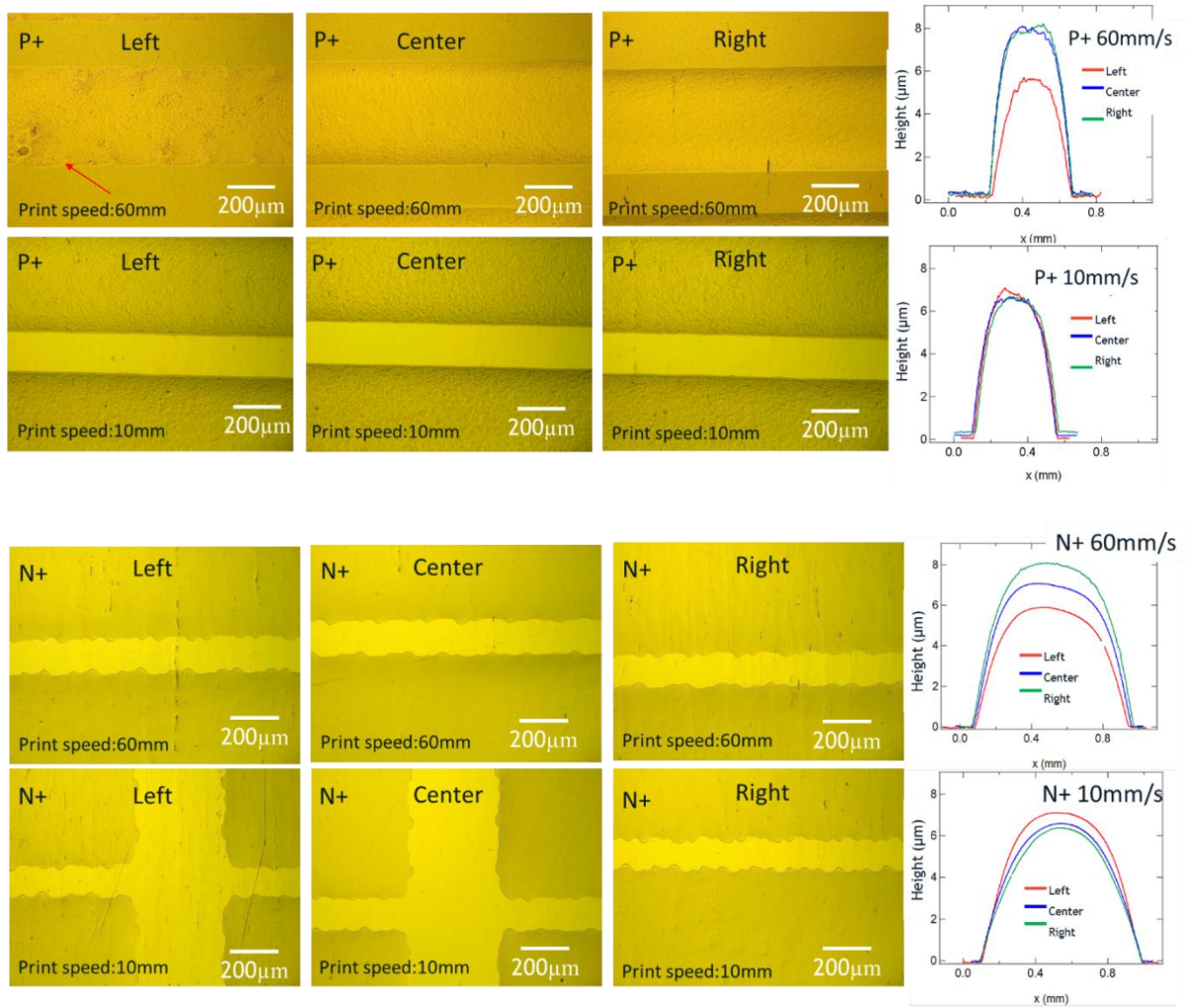


Figure 5.9: Optical microscope image (x250) and cross-section profile of the P+ and N+ inks printed at different print speeds (60 mm/s, 20 mm/s). Left-, center-, and right-side positions. Print gap: 4 mm for P+, 4.5 mm for N+, pressure 9 kg.

3.2.3. Latency

Figure 5.10 shows the effects of latency on the P+ and N+ inks on the screen. Both inks demonstrated a positive correlation between increased latency and increased thickness and surface roughness. The thixotropic nature of the P+ ink helped to achieve clean separations even after the ink had dried. Therefore, it yielded a sharp print image even after 60 minutes of latency. Regarding the N+ ink, drying increased visual tackiness and caused poor snap-off, which caused bridging lines.

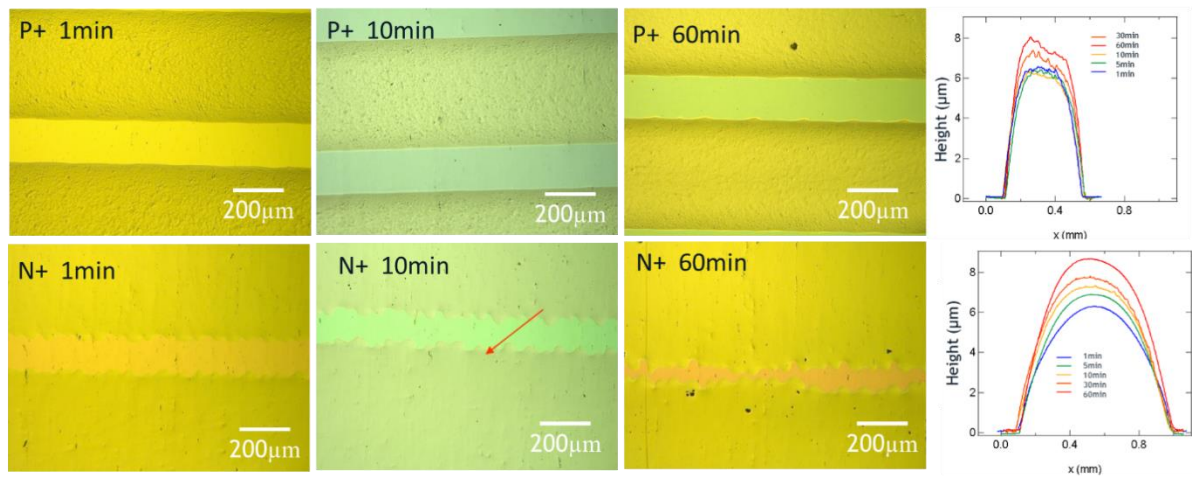


Figure 5.10: Print images of the P+ and N+ inks printed after 1, 10, and 60 min of latency

3.2.4. Optimized condition

The optimized print conditions proved to be flood and print speeds of 20 mm/s, squeegee pressure at 9.0 kg, print gaps of 4.5 mm for the N+ ink and 3 mm for the P+ ink, and a separation speed of 0.5 mm/s. Under the optimized print conditions, both the P+ and the N+ inks were printed with line and space resolutions decreased to 100 μm .

Figure 5.11(a) shows the clean snap-off of the N+ ink under optimized conditions (print speed 20 mm/s, print gap 4.5 mm). Figure 5.11(b) shows an example of a poor snap-off under less-than-optimal conditions (print speed 20 mm/s, print gap 2 mm). The poor separation of the screen from the substrate caused the ink to smudge, and the thicknesses became varied and increased.

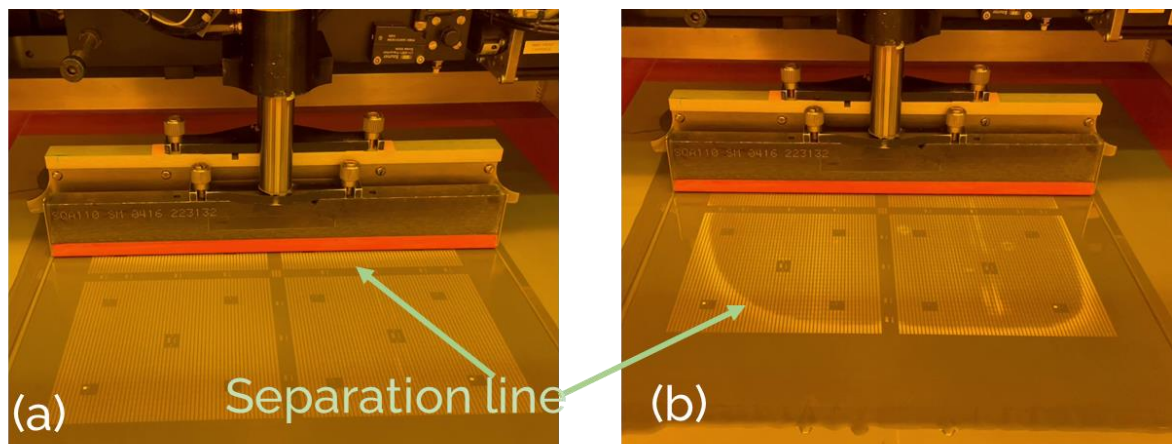


Figure 5.11: (a) Clean snap-off of the N+ ink at optimized conditions (print speed 20 mm/s, print gap 4.5 mm), (b) example of a poor snap-off of the N+ ink (print speed 20 mm/s, print gap 2 mm)

3.3. Activation

3.3.1. Activation temperature skew

Figure 5.12(a) and (b) reveals the sheet resistance of P+ and N+ doped polysilicon at various activation temperatures and durations. The sheet resistance was the lowest at 790 °C and it then varied over 825 °C. The temperature of 790 °C was sufficient to activate both P+ and N+ dopants.

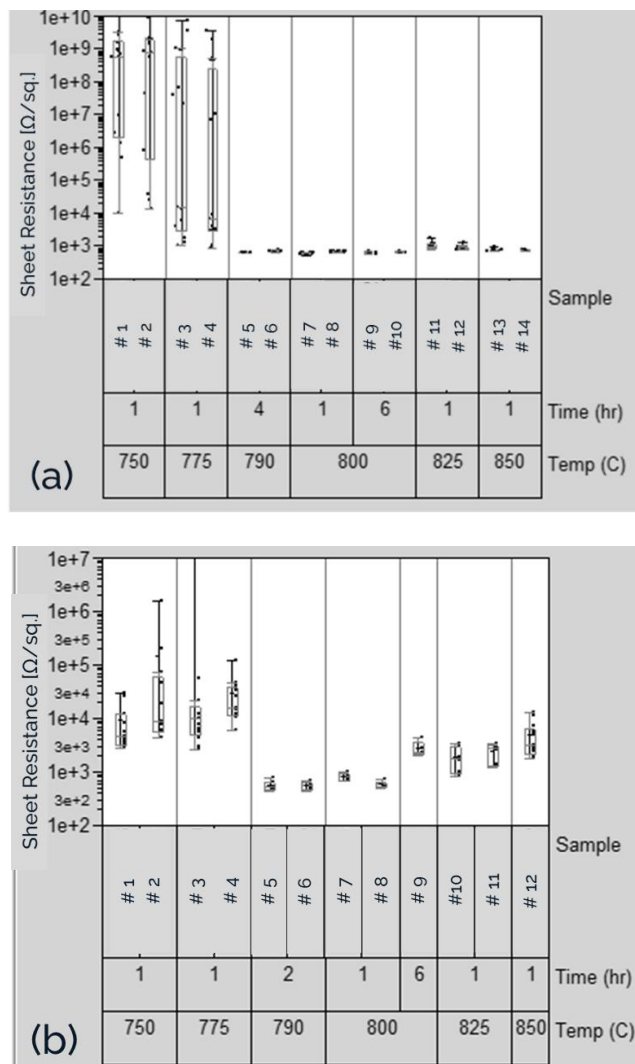


Figure 5.12: Sheet resistance of active layer after activation anneal with (a) P+ ink at various temperatures and durations, (b) N+ ink at various temperatures and durations

3.3.2. P+ ink TMB/SOG vs. pitting

Figure 5.13 shows SEM images of the polysilicon active islands and field oxide layers after P+ ink activation and residue removal using HF acid. Various TMB/SOG ratio compositions were used for the evaluation. When the SOG content was small, pitting of the oxide surface was observed. According to the literature, the etching rate of highly boron-doped SiO₂ with HF acid is faster than it is with low doped SiO₂ [14, 15]. Thus, localized concentrations of boron-doped SiO₂ were etched faster than less concentrated areas, thus causing pitting. In this case, TMB formed B-O-Si bonding with the SOG, so a greater SOG ratio reduced boron migration, which decreased localized concentrations, thus reducing pitting. Thus, the degree of oxide pitting was modulated.

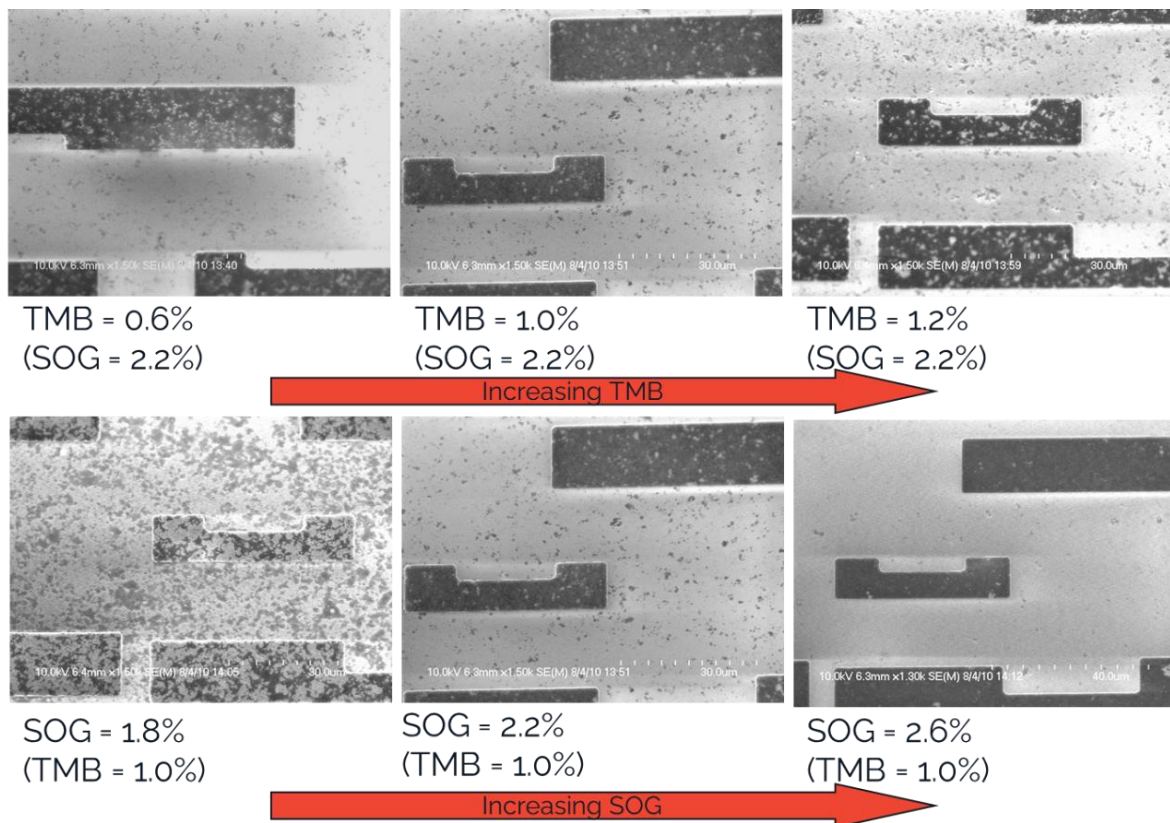


Figure 5.13: SEM images of the P+ ink at various TMB/SOG ratios printed area after residue removal

3.3.3. Dopant concentration skew

Figure 5.14 (a) shows the sheet resistance of P+-doped polysilicon at various ink compositions. Sheet resistance was around 1000 Ω/s , and the TMB composition varied from 0.8–1.2 wt% without impacting activation. Figure 5.14(b) shows the sheet resistance of N+-doped polysilicon at various phosphoric acid concentrations. The resistance decreased by approximately half for every 0.1 wt% increase in ink. Based on the above data, the optimized active ingredient concentration was determined to be 0.5 wt% phosphoric acid in the N+ ink, where sheet resistance was saturated. In the P+ ink, 1.0 wt% of TMB and 2.6 wt% of SOG were used to modulate sheet resistance at around 1,000 Ω/sq , and the pitting was decreased the most.

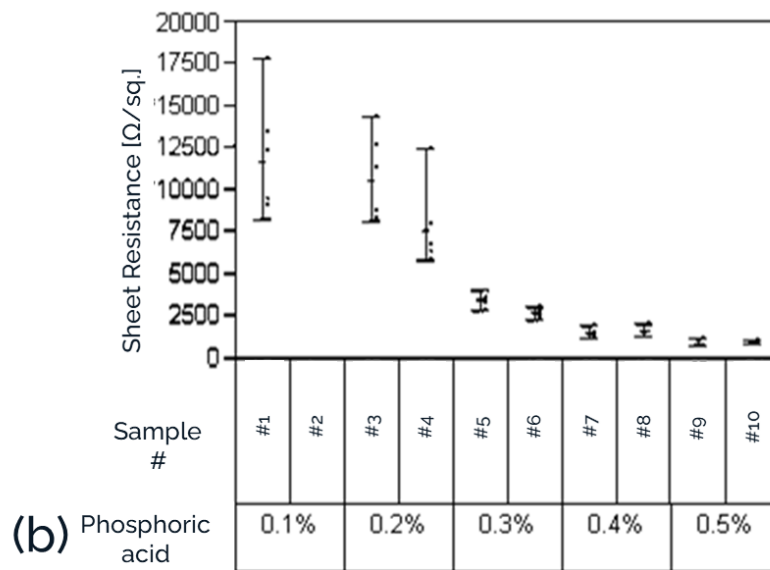
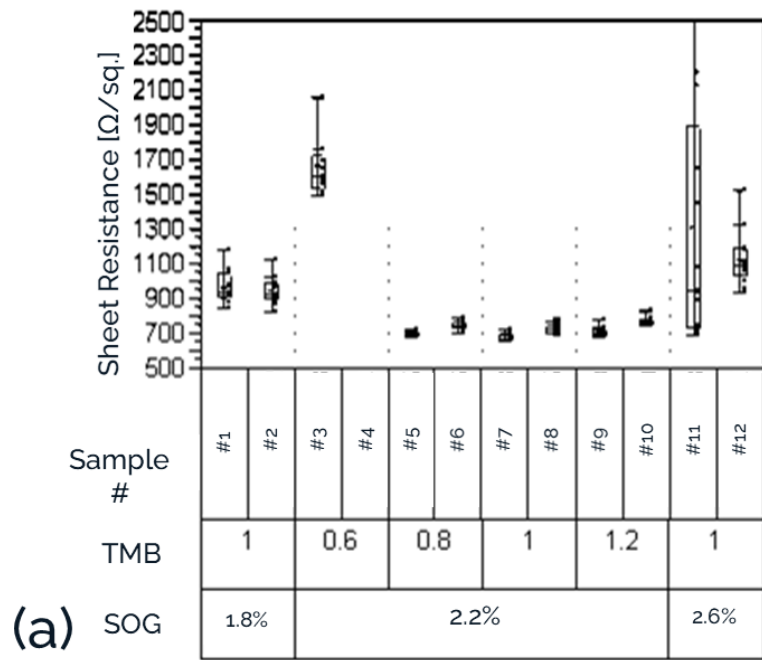


Figure 5.14: Sheet resistance of active layer after activation anneal with (a) P+ ink at various TMB and SOG concentrations, (b) N+ ink at various phosphoric acid concentrations

3.3.5. *Q-time skew*

Figure 5.15 (a) reveals the effects of q-time on the P+ ink before soft baking. Increasing the q-time from printing to soft baking increased resistivity. In the P+ ink, the solvent α -terpineol was relatively hydrophilic. It absorbed moisture, which caused the ink to lose its doping capability when the q-time in air was longer. Therefore, the throughput of the screen printer and the soft bake needed to be matched so that one process could immediately feed the next. The effect of q-time on the N+ ink's sheet resistance, as shown in Figure 5.15(b), before soft baking was negligible compared with that of the P+ ink.

Figure 5.16 shows the effects of q-time between soft baking and activation annealing. In this case, more than 24 hours of q-time was allowable for both the P+ and N+ inks, which made production more manageable compared with the effect of the q-time before soft baking.

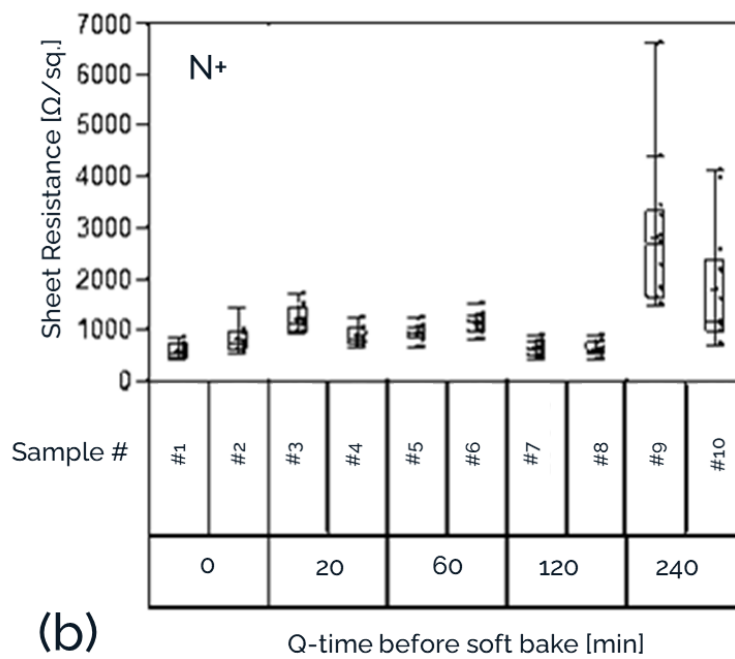
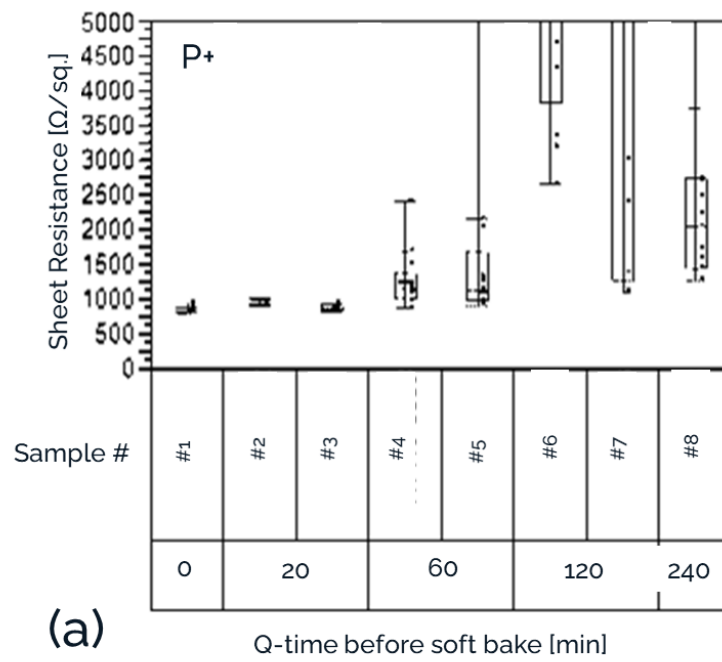


Figure 5.15: Sheet resistance of active layer after activation anneal with (a) P+ ink and (b) N + ink at various q-times before the soft bake

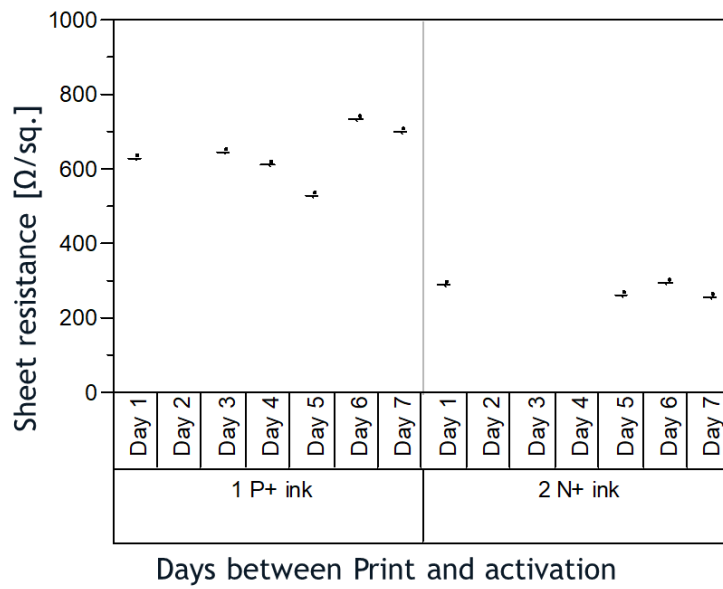


Figure 5.16: Sheet resistance of active layer after activation annealing of P+ and N+ inks according to various days of q-time before activation annealing

3.4 Residue removal

After activation, a black residue was left. Figure 5.17 shows the XPS spectra of the P+ and N+ ink residues after activation annealing. Figure 5.17(a) shows the XPS spectrum of the P+ ink residue, which was a matrix of carbon and B₂O₃. Figure 5.17(b) shows the XPS spectrum of the black residue left by the N+ ink, which contained carbon and white P₄O₁₀. Contrary to our expectations, the carbon did not burn off completely. Si and SiO₂ were expected to be observed in the doping reaction (e.g., P₄O₁₀ + 5Si → 5SiO₂ + 4P), but no SiC or SiN was detected. This black carbon residue was shown to have an important role in preserving the dopant at the silicon interface until the substrate temperature reached 790 °C.

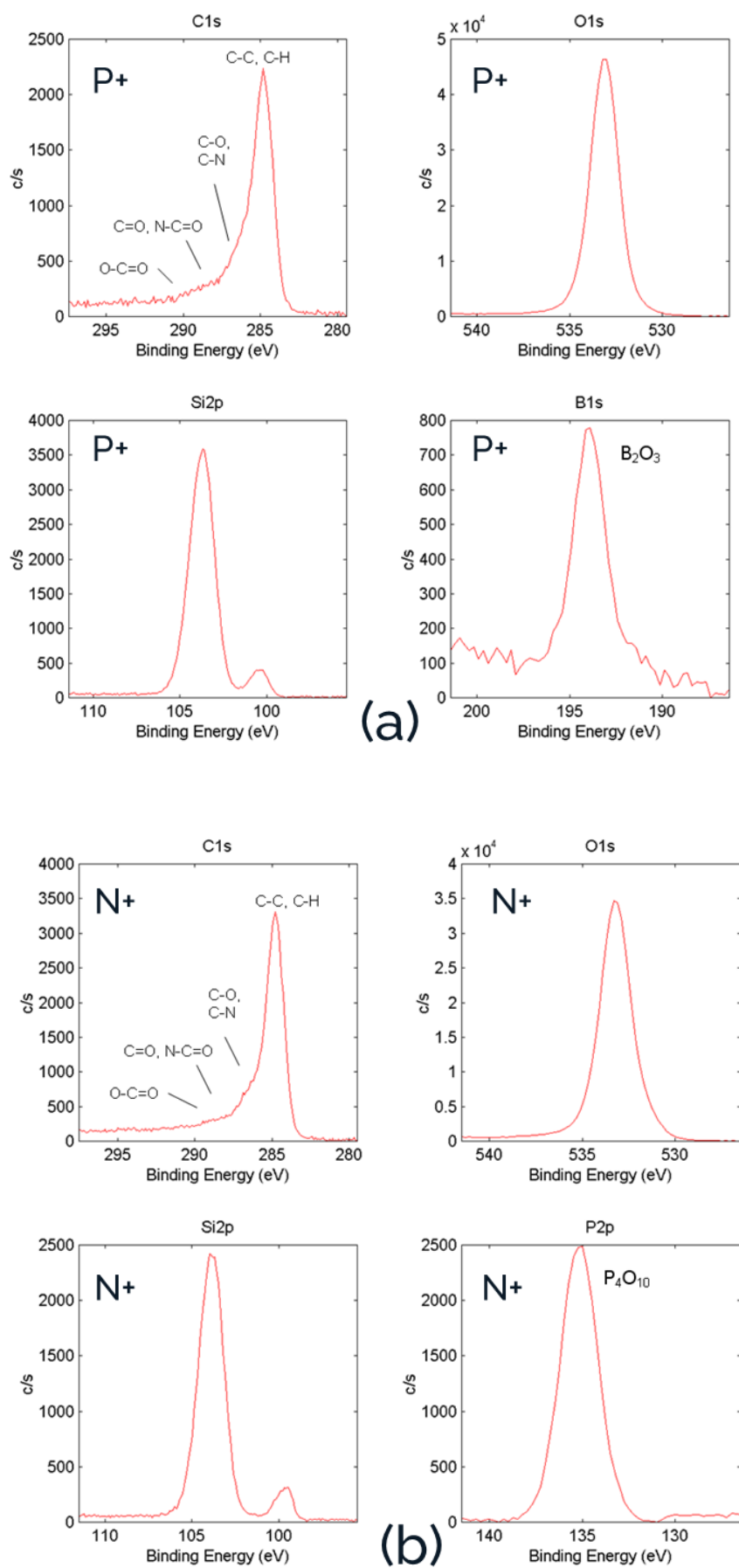


Figure 5.17: XPS spectra of residue of (a) P⁺ and (b) N⁺ inks after activation

The residue of the P+ ink contained carbon and boron oxide, which acted as a dopant, and the black carbon worked as a matrix to preserve the boron at the silicon interface. The carbon was removed using O₂ plasma ash, and the residue was etched off using diluted (500:1) HF acid. Figure 5.18(a) and (d) shows the black residue after activation and Figure 5.18(b) and (f) shows the same surface after O₂ plasma ashing. Figure 5.18(c) and (f) shows the results after the dip in 500:1 HF acid. No trace of the residue was observed after cleaning, which was critical in ensuring smooth topography for the electrical yield and integrity of subsequent films.

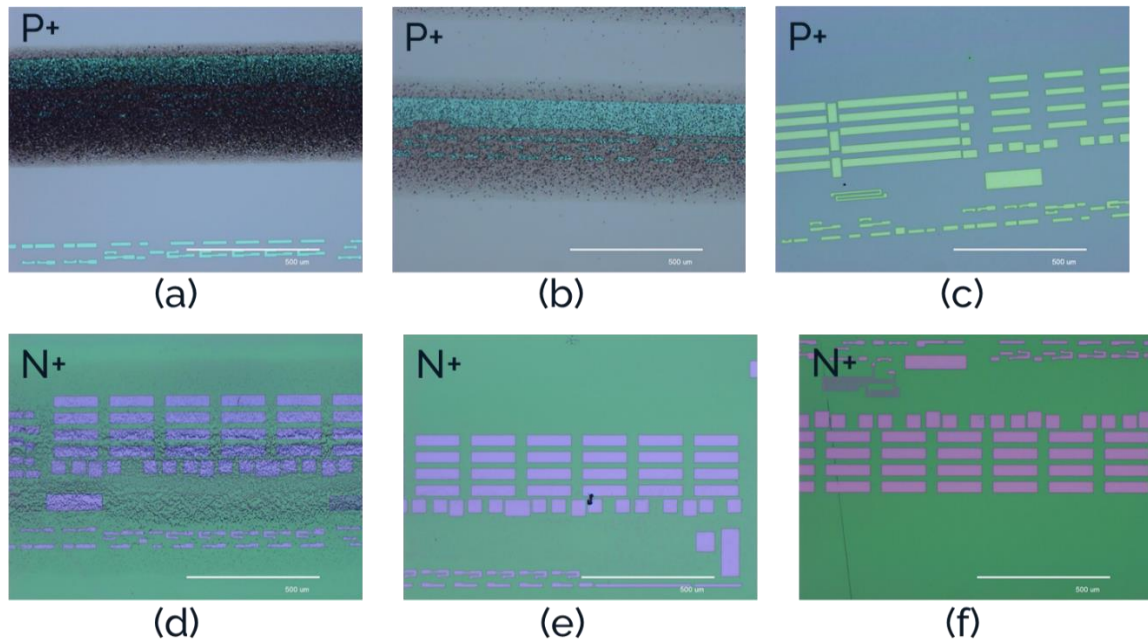


Figure 5.18. Microscope images of (a), (d) residue of P+ ink after activation anneal, (b), (e) after O₂ plasma ashing, and (c), (f) after dipping in 500:1 HF acid solution for 5 min

3.5 Discussion of N+ shorts

In the overall production of TFT, N+ shorts were the major failures. To obtain as much mobility as possible, channels were laid along the direction of grain growth. When the channels were laid perpendicular to grain growth, shorts between the source and drains were not observed, but mobility was reduced. Therefore, it was suspected that the root cause of the N+ shorts was related to diffusion along the grain boundary in the lateral direction, as shown in Figure 5.19.

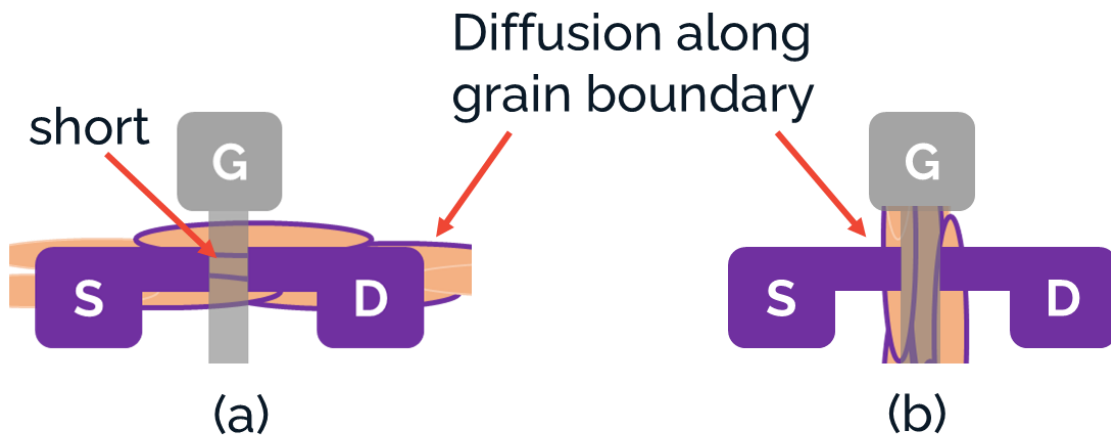


Figure 5.19: The model of shorting along the grain boundary and relation of channel direction: (a) the channel laid in the parallel direction and (b) the channel laid in the perpendicular direction

The source and drain of N+ tended to become shorter compared with P+. Several previous studies have reported that the diffusion of phosphorous was enhanced in the grain boundary and diffused much faster and deeper than when it was segregated. Boron was not segregated at the grain boundaries [20, 21]. The diffusivity of phosphorus at the grain boundary of polysilicon was reported to be $4 \times 10^{-3} \text{ cm}^2/\text{s}$, while the diffusivity of boron was reported to be $6.6 \times 10^{-4} \text{ cm}^2/\text{s}$ using furnace annealing at 1,000–1,200 °C [22]. Therefore, the N+ dopant phosphorous was diffused along the grain and created a path along the grain boundaries, thereby tending to create a short path between the source and the drain.

To suppress the unnecessary diffusion of phosphorous, the following approaches were explored. First, because the diffusion of phosphorous into silicon developed $P_4O_{10} + 5Si \rightarrow 5SiO_2 + 4P$, by adding very thin SiO_2 as a barrier layer using either the vacuum technique or SOG, diffusion was restricted. Another approach was simply to minimize the volume of the printed N+ ink. Figure 5.20 (a) shows the nominal number of shorts with and without 50 Å SiO_2 on the polycrystal island before printing N+ dopant ink. Figure 5.20(b) shows the nominal number of shorts with various printed thicknesses of the N + dopant. In both approaches, the number of shorts was significantly reduced. Maintaining print thickness became vital for TFT fabrication.

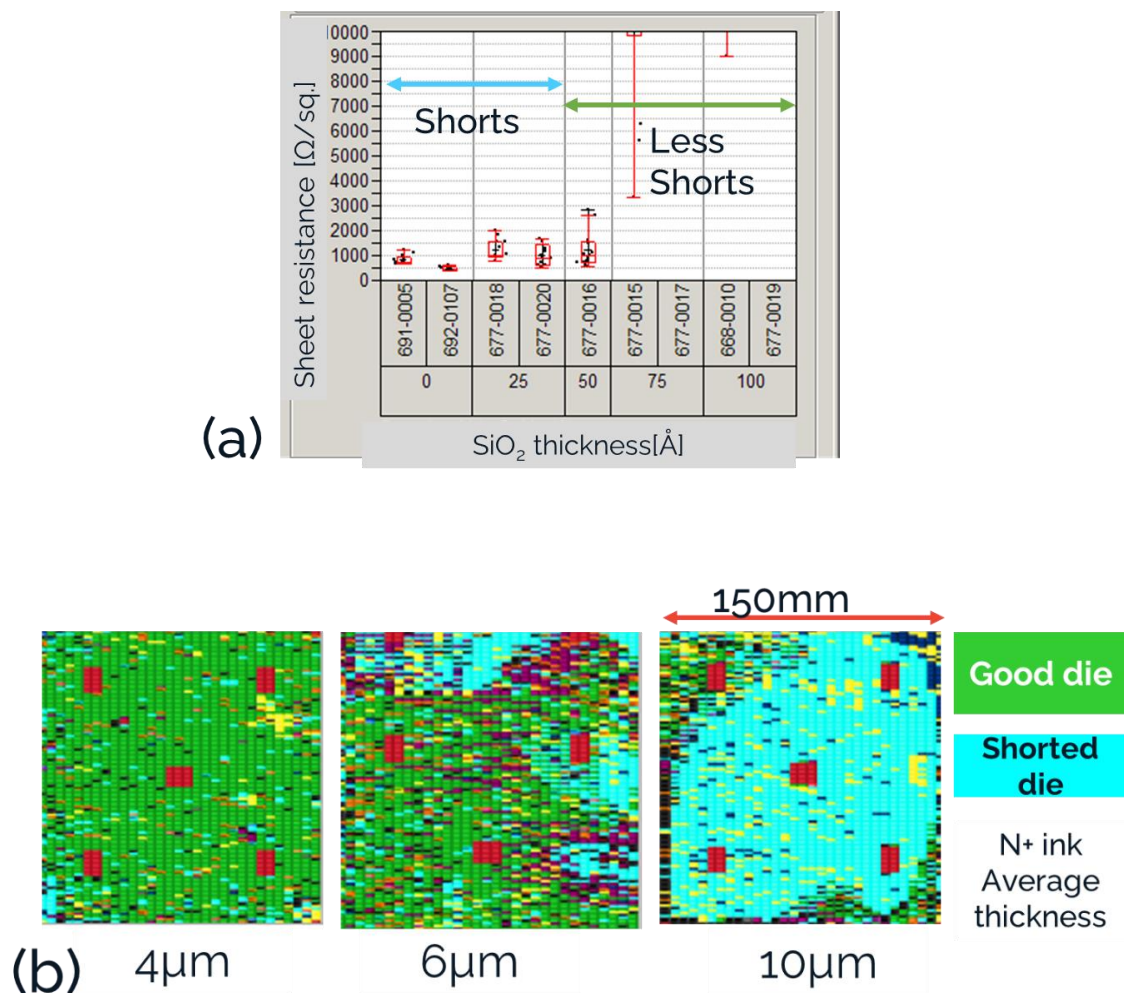


Figure 5.20: Nominal number of NMOS shorts in 300 mm² substrate with (a) various thicknesses of SiO_2 barrier layer before N+ ink print against sheet resistance and shorts, (b) electrical test map of good product dies and shorted dies against various thicknesses of N + ink

4. Conclusion

Novel screen-printable N⁺ and P⁺ dopant inks were studied to fabricate polysilicon thin-film transistors. A solution of poly-IBMA was purified, and the level of trace metals was reduced to less than 20 ppb. TMB and SOG were added to formulate the P⁺ ink, and phosphoric acid was added to formulate the N⁺ ink. The print conditions for each ink were optimized, and the thickness of inks was between 5 and 7 μm . The minimum resolution of line and space was reduced to 100 μm across a 300 mm² stainless steel foil substrate. After thermal anneal activation, sheet resistance was modulated to 200 Ω / sq. for the N⁺ ink and 1,000 Ω / sq. for the P⁺ ink. Q-time in air of the P⁺ ink before the activation of annealing was more than a day without the loss of doping capability, which was sufficient to facilitate manufacturing. After annealing, the residue was removed using a mild process, and the thin silicon layer and gate oxide were undamaged.

The screen printable dopant ink and doping process decreased both the high cost and maintenance of ion-implant equipment in a magnitude order lower cost and maintenance screen printer. Furthermore, the cost of the ink itself was negligible, because most of the content was due to common bulk chemistry. The dopant inks were the first printed process adapted to the volume production of TFT fabrication.

5. References

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Chapter 6

Consideration of Roll-to-roll and Polytetrasilane Ink

1. Introduction

In the hybrid process, three fundamental technologies were successfully used to establish the volume production of logic circuits using polysilicon TFTs. However, our final goal was to increase the scale to produce billions of products at very cost. To achieve this goal, roll-to-roll manufacturing was planned. I learned that the scale and supply of silicon ink were a bottle neck. In this chapter, a methodology based on sensitive electrical characterization and optical inspections is applied to evaluate the suitability of a process for moving from sheet-based to roll-to-roll-based production. Additionally, low-cost silicon ink, which was newly synthesized, was tested by fabricating TFTs compared with poly-CPS.

2. Experiments

2.1. Roll to roll

2.1.1 Simulated bend stress

A particular concern regarding flexible substrate manufacturing in moving from sheet-based to roll-based production is layer integrity during the bends around machine rollers. Potential stress cracks and internal film stresses may impact the reliability and performance of devices. To simulate the impact of rollers and bending stress on device characteristics, substrates with large area capacitors and polysilicon TFTs were wound around rollers of successively decreasing diameters of 6 inches, 3 inches, 1.5 inches, and 0.75 inches for durations ~10

seconds. The electrical characteristics of the device were obtained after each bend. Figure 1 shows an example of devices bent around a 3-inch and 1.5-inch roller.

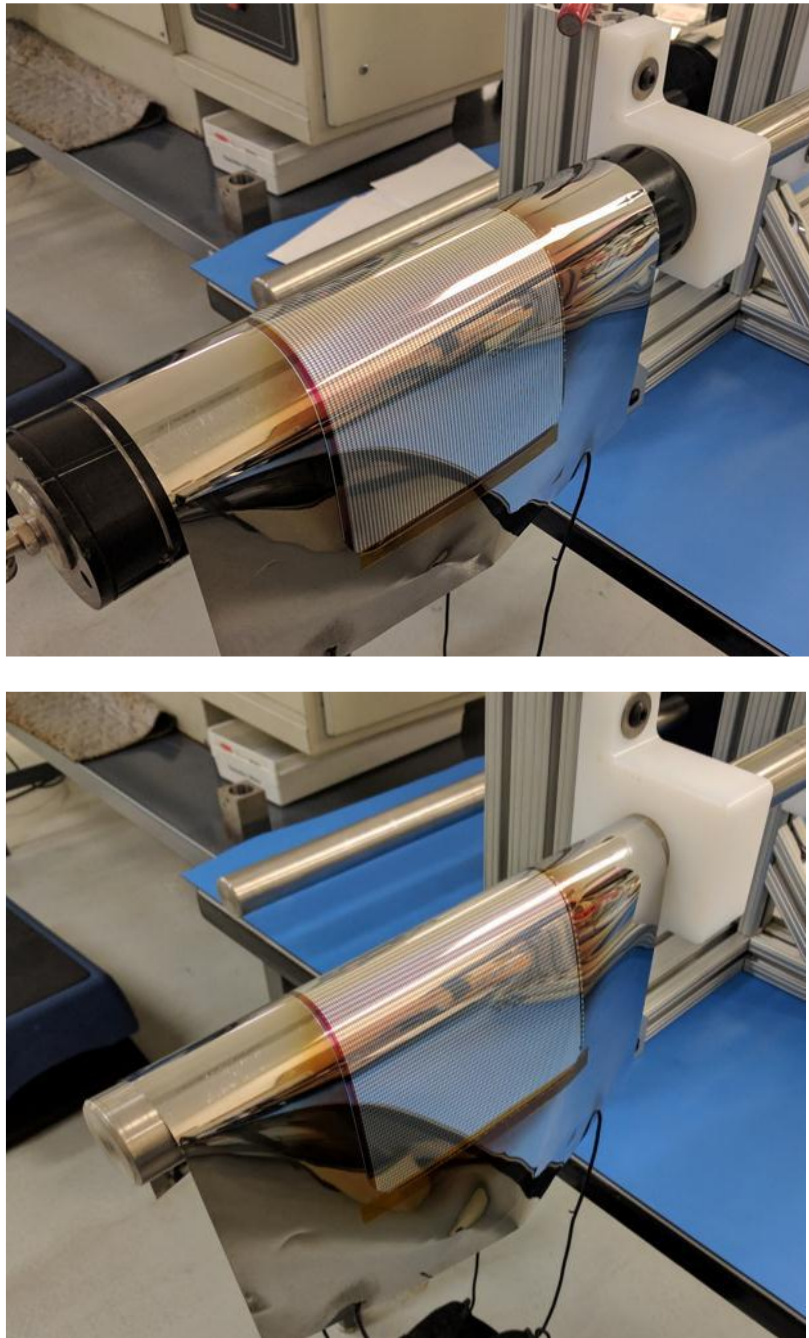


Figure 6.1: Bending of active devices around rollers (a) 3 inches in diameter and (b) 1.5 inches in diameter.

2.2.2 Capacitor fabrication

Large area metal-insulator-metal (MIM) capacitors (2 mm x 1 mm wide), as shown in Figure 6.2, were fabricated on 100 μm thick 300 mm² stainless steel using refractory metal layers and dielectrics. Leakage current values at 7 V were obtained with an HP4155 Analyzer after each bend stress on two sheets, each of which contained more than 8,000 MIM devices. No measurable change in capacitor behavior was detected electrically, as shown in Figure 7.3. Optical inspections also showed no evidence of stress cracks due to bending.

In conclusion, a comparison of substrates and a methodology for evaluating risks in moving from a sheet-based process to a roll-to-roll-based process was conducted. Sensitive electrical measurements of TFT and MIM capacitors allowed for the early evaluation of potential challenges when devices were wound over multiple bend rollers.

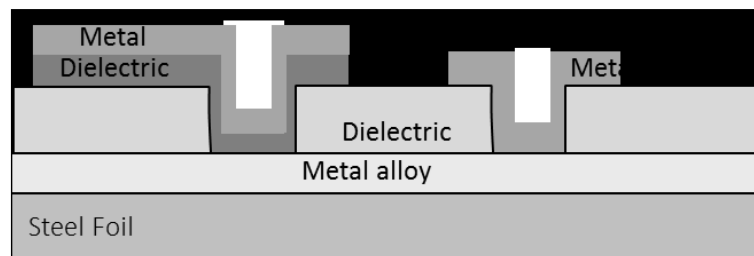


Figure 6.2: Cross-section of the metal-insulator-metal (MIM) capacitors on stainless steel foil

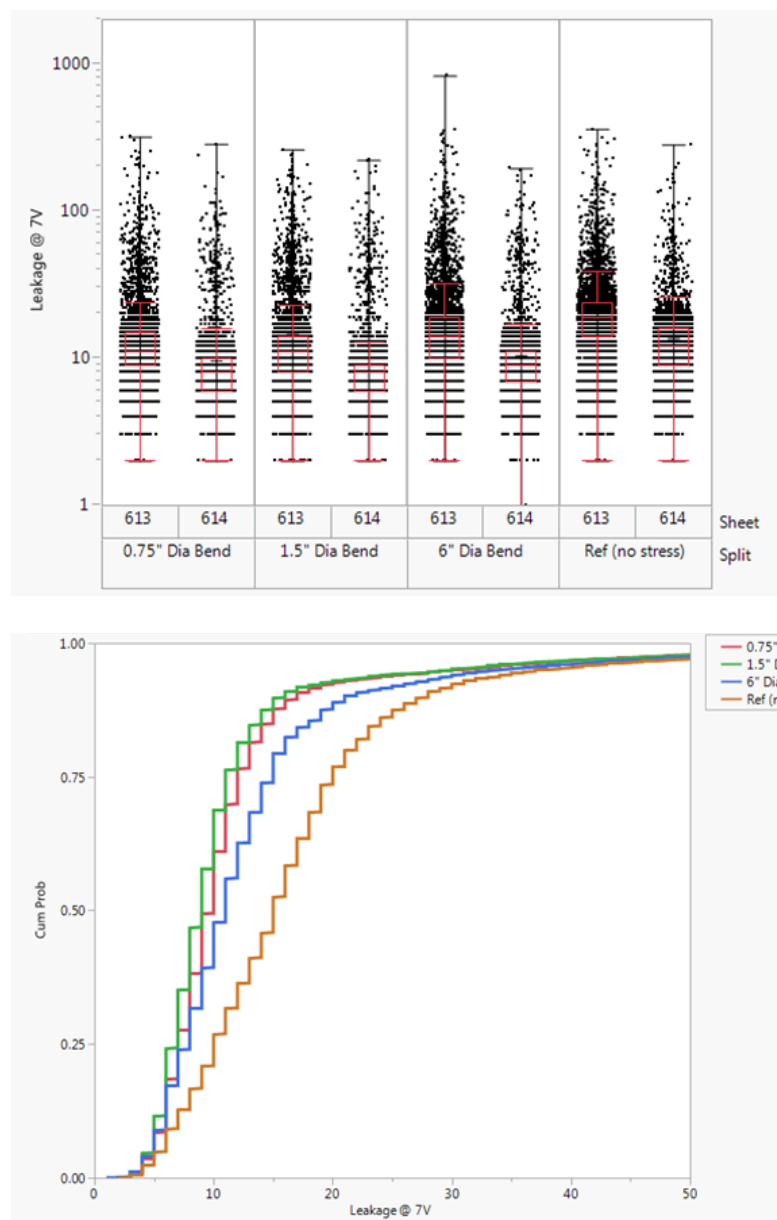


Figure 6.3. Leakage values pre- and post-bending stress. Sheets 1 and 2 were identically processed.

2.2. Polytetrasilane ink

In previous studies, the fabrication schemes of polysilicon TFTs were developed using inkjet printed and slot-die coated CPS-based silicon ink. It was shown that high-quality polysilicon film, which is equivalent to low-temperature polysilicon via PECVD, can be fabricated using CPS-based ink.

However, the synthesis of CPS, as proposed by Hengge et al. in the 1980s ^[1], requires multi-step reactions, as shown in Figure 6.4 (a). Additionally, multiple distillation, filtering, and washing are required, depending on the purification strategy. Furthermore, most of these operations require a complicated setup in glove boxes because silanes and lithium are pyrophoric when they react rapidly with oxygen. To synthesize poly-CPS, an additional polymerization step was also required, using a proprietary heterogeneous catalyst based on platinum group metal. Furthermore, in the last decade, the cost of lithium and platinum group metals has risen because of their increasing use in industry. The complex synthesis and rise in material costs have created major bottlenecks in the supply and use of CPS-based ink.

Consequently, to simplify the synthesis of silicon precursors, we developed a polymerization process ^[2,3] to produce normal monomer silanes, such as n-tetrasilane and n-trisilane, using a proprietary heterogeneous catalyst, as shown in Figure 6. (b). Semiconductor-grade n-tetrasilane and n-trisilane are commercially available, and the heterogeneous catalyst synthesized in-house was made from a common metal. The synthesis scheme involved single-step polymerization and filtering. Because of the simplicity of formulating this ink, it would be easy to scale in the future at a reduced cost.

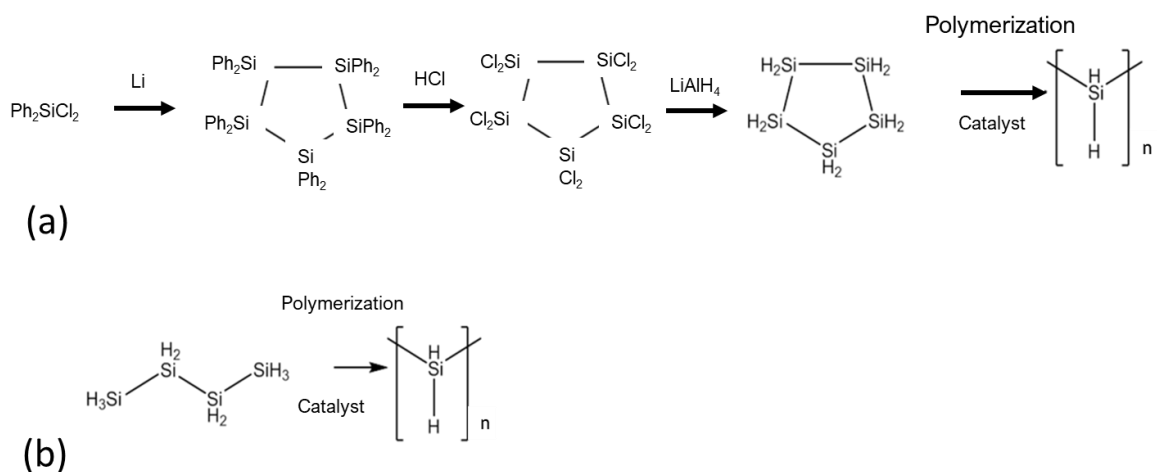


Figure 6.4: Synthesis path of (a) poly-CPS and (b) polytetrasilane

In this study, amorphous silicon films were formed using spin-coated poly-CPS and polytetrasilane inks. The laser was then crystallized and compared with polysilicon film via PECVD.

To prepare the ink, the molecular weights of poly-CPS and polytetrasilane were modulated to be low enough to dissolve in a solvent. The solvent required for formulating the inks needed to be transparent and inert under UV irradiation. Moreover, it could not have an oxygen constituent, as any peroxide or oxygen radicals would react with the silane. Cyclooctane, which is cycloalkane (boiling point $\sim 150\text{ }^{\circ}\text{C}$), was chosen as the solvent to use in the spin coating. The cyclooctane was purified to remove oxidizing compounds that would have contaminated the silicon film, thus reducing carrier mobility.

Because the spun film of both poly-silanes would migrate under heat, they were simultaneously UV-treated during their spin prior to baking to increase their molecular weight. By increasing their molecular weight and crosslinking, the wet films were stabilized into heat-resistant soft polymers. As Gerwig et al. demonstrated, UV irradiation cleaved Si-Si bonds, generating-Si radicals and radical reactions in which higher molecular weight silane polymers could be generated ^[4].

The spun films were baked at 400 °C in ambient nitrogen to convert them to amorphous silicon films^[5]. Then, to crystallize the active islands, a solid-state green (532 nm) laser was chosen because of its stability and low cost of operation.

The inks were prepared as follows. The CPS was synthesized using the modified Hengges' scheme shown in Fig 6.4 (a) and purified in-house. The n-tetrasilane was obtained from Voltaix (Gelest). The monomer silanes were polymerized using proprietary catalysts that were synthesized in-house. The molecular weight was monitored during polymerization using gel permeation chromatography (GPC, 0.5 wt% in cyclohexane; no reference polymer was added). The polymerization was terminated when the desired molecular weight was reached. The resulting polymer was analyzed using proton nuclear magnetic resonance (¹H-NMR, 500MHz, Cyclohexane-d₁₂: Aldrich, 99.6 atom%D, no internal standard). Cyclooctane (> 99%, Sigma-Aldrich) was used as the solvent. It was washed using sulfuric acid (Sigma-Aldrich) and then distilled over sodium (Sigma-Aldrich) to remove any remaining traces of water. Poly-CPS and polytetrasilane were added at 15 vol% in preparation for spin coating.

A Laurel spin coater was set up in a Mbraun glove box in ambient nitrogen. A grid low-pressure mercury lamp (Jelight) and exhaust were integrated into the lid of the spin coater. Silicon wafers 100 mm in diameter at the base were cleaned and thermally oxidized, which resulted in a 1-μm SiO₂ film as the field oxide. The inks were dispensed at 1 ml each using a glass syringe through a 0.2 μm PTFE disk filter on an SiO₂ coated silicon wafer. After a short spreading rotation at 500 revolutions per minute (rpm) for 5 s, a high-speed rotation at 1,000 rpm was introduced with simultaneous UV irradiation and exhaust. The coated silane polymer film was then baked in a muffle oven under nitrogen gas flow via a gas purifier at 400 °C for 20 min to reduce the hydrogen. The wafers were then subjected to a dehydrogenation bake at 550 °C for 12 hours. The incorporated impurity levels of the spin-

coated film were determined using secondary ion mass spectroscopy (SIMS). All operations were performed in a glove box that maintained oxygen and moisture levels below 5 ppm.

At this point, an amorphous silicon film deposited via PECVD was introduced as a second control. A top-gate, self-aligned process flow using an aluminum gate and ion implantation was used for doping. The three dehydrogenated amorphous silicon films were crystalized using a solid-state laser (531 nm, 1300 mJ/cm²).

The resulting polysilanes were analyzed by ¹H-NMR and GPC before and after polymerization. Figure 6.5 (a) shows ¹H-NMR spectra of CPS. Single peaks were without splits because the CPS protons were identical and equivalent in their magnetic orientations. Regarding spin–spin coupling from the possible proton magnetic orientations, for n-tetrasilane, the interactions of non-equivalent protons on adjacent silicon atoms were considered. Figure 6.5(b) shows the spectrum of n-tetrasilane and the peaks of SiH₂ and SiH₃. SiH₂ protons were split by SiH₃ protons into a 1:3:3:1 quartet. SiH₃ protons were split by SiH₂ protons into a 1:2:1 triplet. The peaks observed between 3.0–3.5 ppm were not symmetrical and suggested overlaps of peaks of SiH₂ and SiH₃.

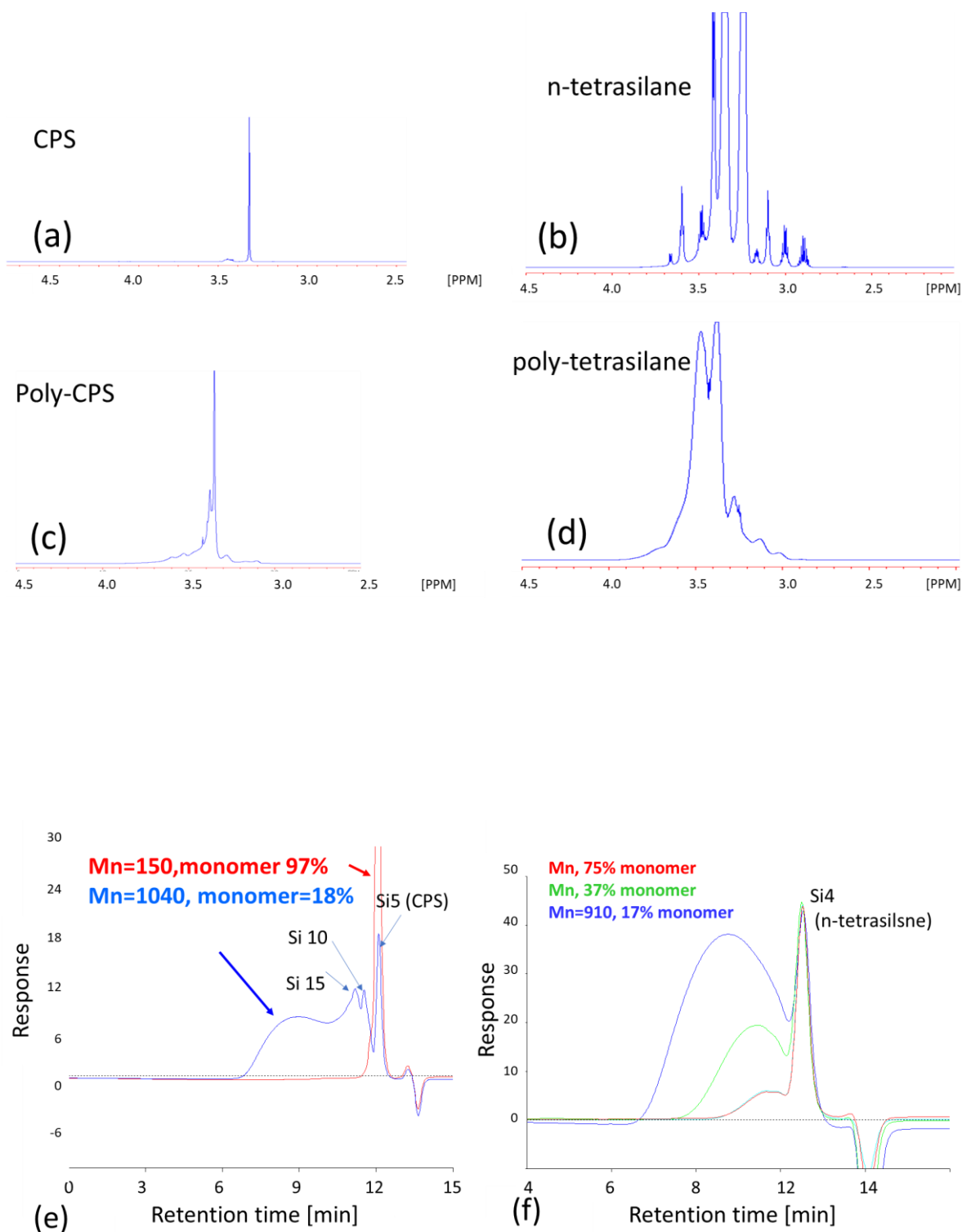


Figure 6.5: ^1H -NMR spectra of (a) CPS, (b) n-tetrasilane, (c) poly-CPS, (d) poly-tetrasilane, and GPC spectra of (e) CPS and poly-CPS, and (f) n-tetrasilane and polytetrasilane

Figure 6.5(c) shows sharp peaks and broad peaks of the poly CPS ^1H -NMR spectrum. The broad peaks exhibited splits of various proton statuses of leaner and isopolymers. The sharp peaks represented dimers or trimers. These were also observed in GPC, which suggested that a CPS proton was pulled off and then generated Si_5H_{10} with a radical before forming a bicyclic dimer or trimers. Gerwig et al. presented a bicyclic dimer model as result of UV-induced polymerization [4]. Another hypothesis regarding the open-ring reaction due to cleaving of the Si-Si bond was stated by Shimoda et al. Figure 6.5(c) shows the NMR spectrum of the polymerized CPS without clear splits. The broad spectrum of polytetrasilane shown in Fig. 6.5(d) shows many splits that were leaner or isopolymers with various proton statuses.

Figure 6.5(e) and (f) shows the GPC spectra of poly-CPS and polytetrasilane. The molecular weight was modulated at approximately $M_n = 1140$ g/mol for poly-CPS and $M_n = 910$ g/mol for polytetrasilane. The shelf life of the formulated ink exceeded several months with no change in appearance or viscosity when it was stored below -20°C . Table 1(a) shows the trace metal impurity of poly-CPS and polytetrasilane measured by ICPMS. The levels of the trace metals were less than those of ppb in both polysilanes. A typical hard-cured film was analyzed using SIMS, and the findings indicated that it contained minimal quantities of carbon, oxygen, and other impurities, as shown in Table 1(b). The carbon levels in the films formed with poly-CPS and polytetrasilane were equivalent to the carbon level of films formed with monomer CPS. This finding indicated that black carbon, which was used to synthesize the catalyst, was completely removed. The level of impurity in polytetrasilane was equivalent to that in poly-CPS, which was already demonstrated to provide an amorphous silicon film equivalent to PECVD.

Table 1. (a) ICPMS of poly-CPS and polytetrasilane. and (b) SIMS analysis of amorphous silicon film deposited via PECVD, poly-CPS, and polytetrasilane

(a)

Atom	Al [ppb]	Ca [ppb]	K [ppb]	Na [ppb]	Mg [ppb]	Li [ppb]	Cr [ppb]	Cu [ppb]
poly-CPS	<0.5	<0.5	<1	6.5	<0.5	<0.5	<0.5	<0.5
polytetrasilane	<0.5	<0.5	<1	2.7	<0.5	<0.5	<0.5	<0.5

(b)

Precursor	C [%]	H [%]	O [%]	N[ppm]	Al [ppm]	Na [ppm]	K [ppm]
CPS	0.04	9.8	0.02	20	0.003	0.002	0.002
poly-CPS	0.04	14.8	0.02	20	0.04	0.02	0.04
polytetrasilane	0.02	12.3	0.02	4	0.05	0.03	0.08

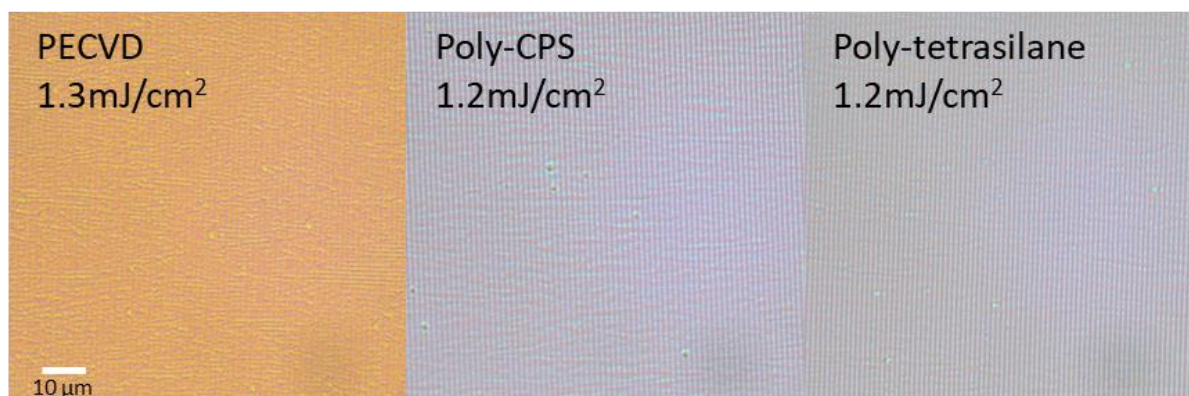


Figure 6.6: Optical microscope images of laser crystallized polysilicon film formed via PECVD, Poly-CPS, polytetrasilane

Figure 6.6 shows a comparison of optical scope images of laser crystallized film. None of the films showed major defects caused by the optimized dihydrogen bake. Lateral crystalline growth was observed on all films, while the PECVD film showed the most obvious

crystalline growth. The results showed that polytetrasilane ink hard baked on the hotplate replaced silicon deposited via PECVD, demonstrating the future potential of low-cost silicon ink in printed electronics.

In this study, polysilicon films were fabricated using spin-coated silicon ink formulated with polytetrasilane synthesized via novel single-step polymerization using a catalyst. Polytetrasilane was synthesized by the polymerization of semiconductor-grade n-tetrasilane using a heterogeneous catalyst and then formulated as silicon precursor ink. The simplicity of polysilane synthesis would solve bottlenecks in supply and the use of CPS-based silicon ink. The results of many previous studies in chapter 4 that used poly-CPS could be reproduced using polytetrasilane. The labor/hour cost of synthesizing polytetrasilane was estimated to be one-third to one-fourth that of synthesizing poly-CPS.

3. Conclusion

In shifting from a sheet process to a roll-to-roll process, production volume increased from 10s of millions to billions per year. In this chapter, damage to a capacitor fabricated on stainless foil was studied under bending conditions running through a roll-to roll line. The results showed that the damage was negligible, demonstrating that our polysilicon TFTs could be fabricated using roll-to-roll equipment.

The supply of silicon ink was a major bottleneck in the printing process. The new synthesis scheme could provide more researchers and manufactures opportunities to access silicon ink.

4. References

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Chapter 7

Conclusion

1. TFT fabrication scheme

To fulfill the promise of moving printed electronics in the laboratory to their production in volume required a new approach that would eliminate inkjet printing and enable hybrid printing using conventional technology. First, a stainless steel foil substrate that was compatible with high temperature processing was developed to place on silicon wafers. Second, screen printing was developed for doping, and third, slot die coating of silicon ink was developed to form the active layer. In this chapter, the above three fundamental technologies were integrated into hybrid process flow to fabricate CMOS polysilicon TFTs. Approximately 13,000 newly designed NFC circuits were fabricated on 300 mm² stainless steel foil substrate, and the TFT characteristics were evaluated. A CMOS polysilicon TFT fabrication process was first established using a silicon layer deposited via PECVD as the control. Then, a silicon layer was deposited using a slot-die coating. Figure 7.1 shows a self-aligned top-gate polysilicon CMOS TFT structure adopted for fabrication. N⁺, P⁺, and passivation inks were printed by screen printing. Four other layers were patterned using a conventional lithography process. Table 6.1 shows the proposed hybrid process of print flow using conventional semiconductors. The flow required four masks and three screen masks. Laser ablation of 128-bit fuses was used in one-time programming.

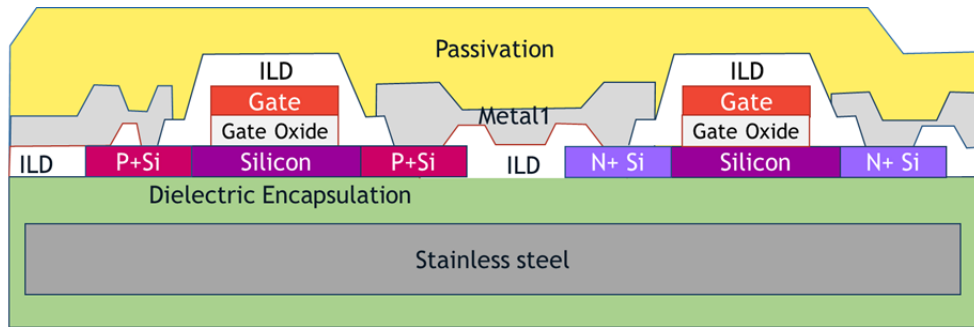
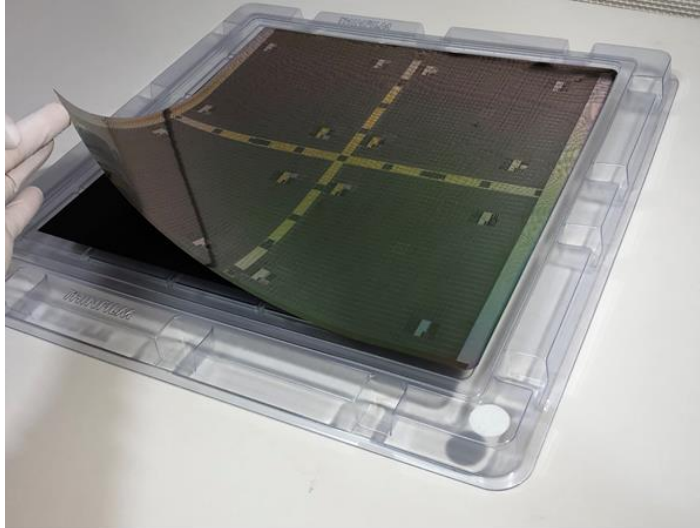


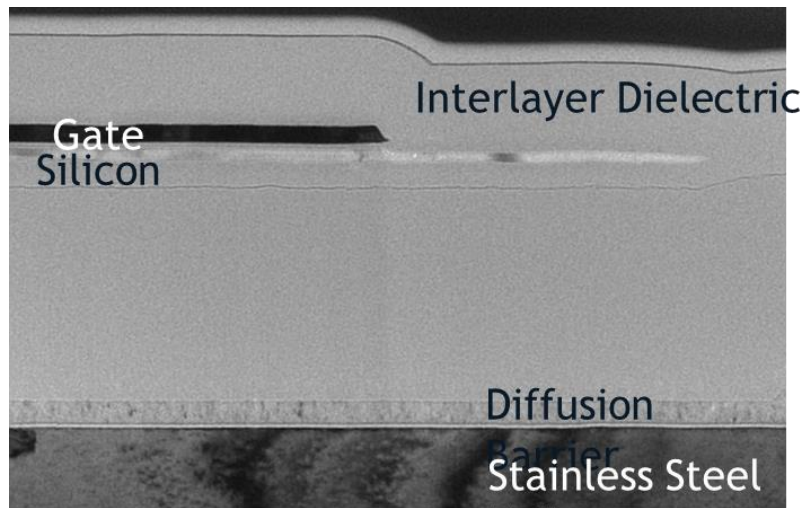
Figure 7.1: Cross-section of CMOS TFTs (not to scale)

Table 7.1: Scheme of the print-conventional hybrid process for the fabrication of CMOS TFTs

Step	Function	Manufacturing Process
1	Substrate preparation and dielectric coating	Blanket coating
2	Form slot-die silicon and pattern active island	Blanket coating + mask1
3	Deposit and pattern gate electrode/dielectric	Blanket coating + mask2
4	Dope source and drain (N+ and P+)	Additive (screen print)
5	Form interlayer dielectric	Blanket coating + mask3
6	Form metal interconnect	Blanket coating + mask4
7	Form passivation	Additive (screen print)



(a)



(b)

Figure7. 2: (a) Finished NFC (13.56 MHz) RFID devices fabricated on a 300 mm x 300 mm x 100 μm stainless steel foil substrate, (b) cross-section TEM picture of encapsulation layer and transistor

2. Conclusion

Simple function devices are essential for the IoT. Fabrication techniques that drive the mega volume production of such devices while decreasing environmental load have been investigated in recent years. The adaptation of printed electronics to flexible substrates has been considered.

In this study, silicon precursors, CPS inks, and other novel inks were developed to achieve a performance that was higher than that achieved by organic semiconductors and metal oxides. The polysilicon films developed in this study were comparable to conventional low-temperature polysilicon using CPS in a manufacturing environment. Furthermore, as a practical solution for the mass production of 13.56 Hz NFC circuits, we developed stainless steel foil substrates that enable high-temperature processes and P⁺ and N⁺ doping by screen printing. These are novel means of forming TFT using a hybrid process of printing and conventional semiconductors, which can be applied to a large area using slot dies.

The production of polysilicon devices using the printing method has progressed greatly from the laboratory stage to mass production, in terms of reducing the cost of devices. Products such as NFC-ID tags and sensor tags are shipped to customers commercially, and they have long contributed to the authentication of products, communication with consumers, and the management of logistics.

As shown in Figure 7.5, stainless steel foil, CPS-based silicon ink, and printed N⁺ and P⁺ dopants can be used in the volume manufacturing of a variety of products to be shipped commercially. TFTs can be applied in the production of signage, large-area sensors, and so on. The use of stainless steel foil could be expanded to many applications that require thin and flexible forms using high-temperature processes, such as micro electro-mechanical systems (MEMS), batteries, and sensors. Silicon ink can be used as a battery anode. Dopant inks can be used in PVs.

The successful results of the study on sheets demonstrated the potential of roll-to-roll volume manufacturing of logic circuits using polysilicon TFTs, which have low energy and material consumption and huge reductions in CO₂ emission. Figure 7.3(a) shows the estimates of energy and material consumption. Figure 7.3(b) shows CO₂ emissions by the same limited function (NFC) chip logic circuit on a 0.18- μ m silicon wafer fabricated by the hybrid printing process on a stainless steel foil sheet compared with the roll-to-roll process. A decreased step count and a lower class of clean rooms contribute to reducing consumption.

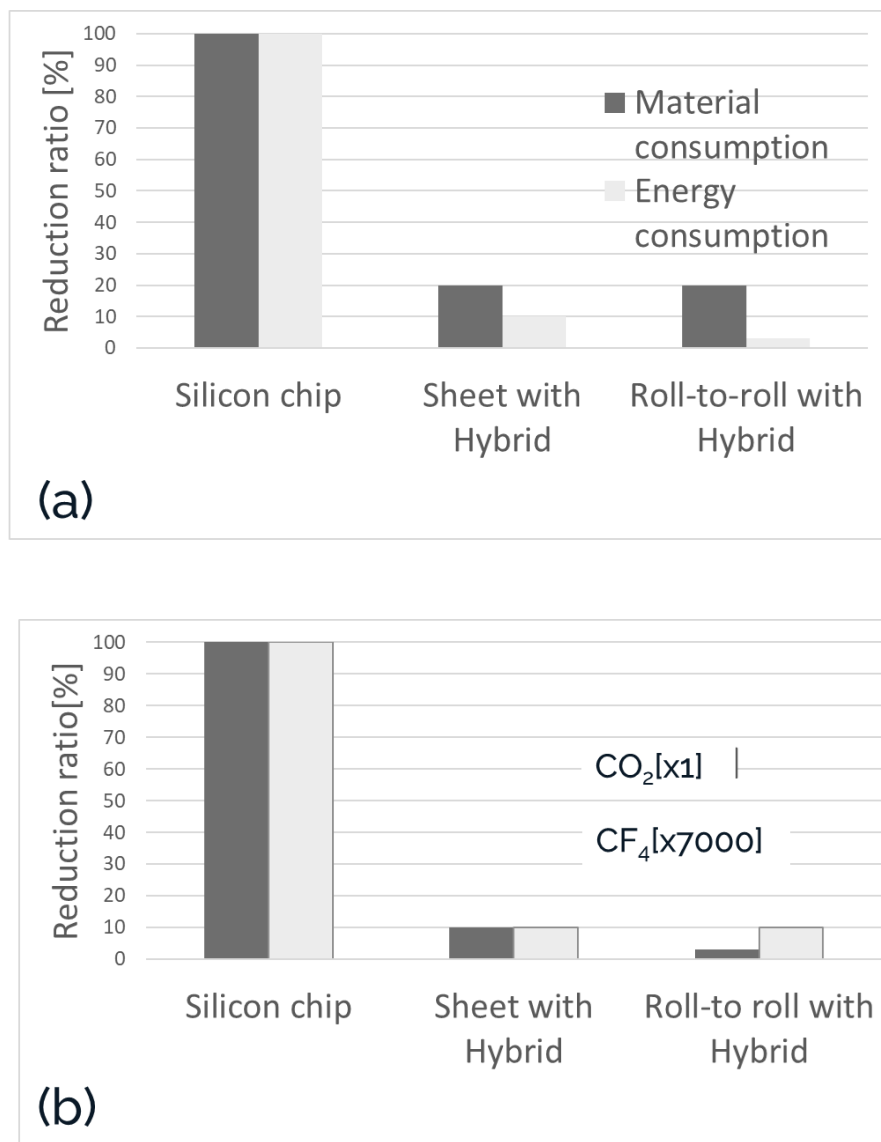


Figure 7.3: Estimated reduction in (a) energy and material consumption and (b) CO₂ emission compared with the 0.18 μ m rule silicon wafer fab against stainless steel foil sheet and roll-to roll.

3. Appendix

3.1 TFT characteristics

Table 7.2: Typical TFT average parameters of PECVD and ink-based transistors with printed dopant on 300 mm x 300 mm x 100 μm stainless steel substrate

TFT type	PMOS		NMOS	
Film deposition method	PECVD	Ink	PECVD	Ink
Mobility sat [cm^2/Vs]	80	80	200	200
Threshold Voltage[V]	-0.6	-0.8	1.0	1.0
Slope [V/decade]	0.25	0.25	0.25	0.25
On/Off	1.0E+07	1.00E+07	1.00E+07	1.00E+07

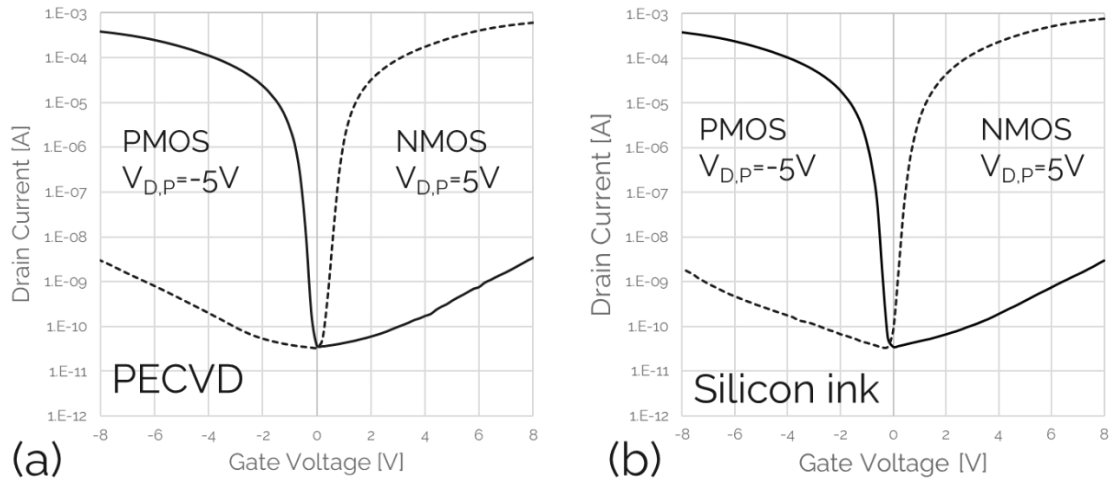


Figure 7.4: Id-Vg characteristics of PMOS and NMOS TFTs fabricated using polysilicon via (a) PECVD and (b) silicon ink, Output of PMOS

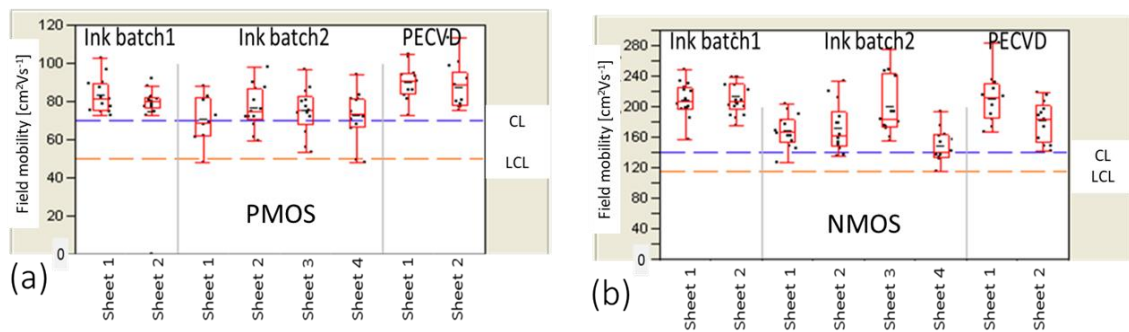


Figure 7.5: Variability chart mobility of (a) PMOS and (b) NMOS TFT devices prepared with ink-based silicon film from multiple ink batches and PECVD methods

3.2 NFC products

Figure 7.6 shows a variety of NFC products, both post assembly and finished as commercial products

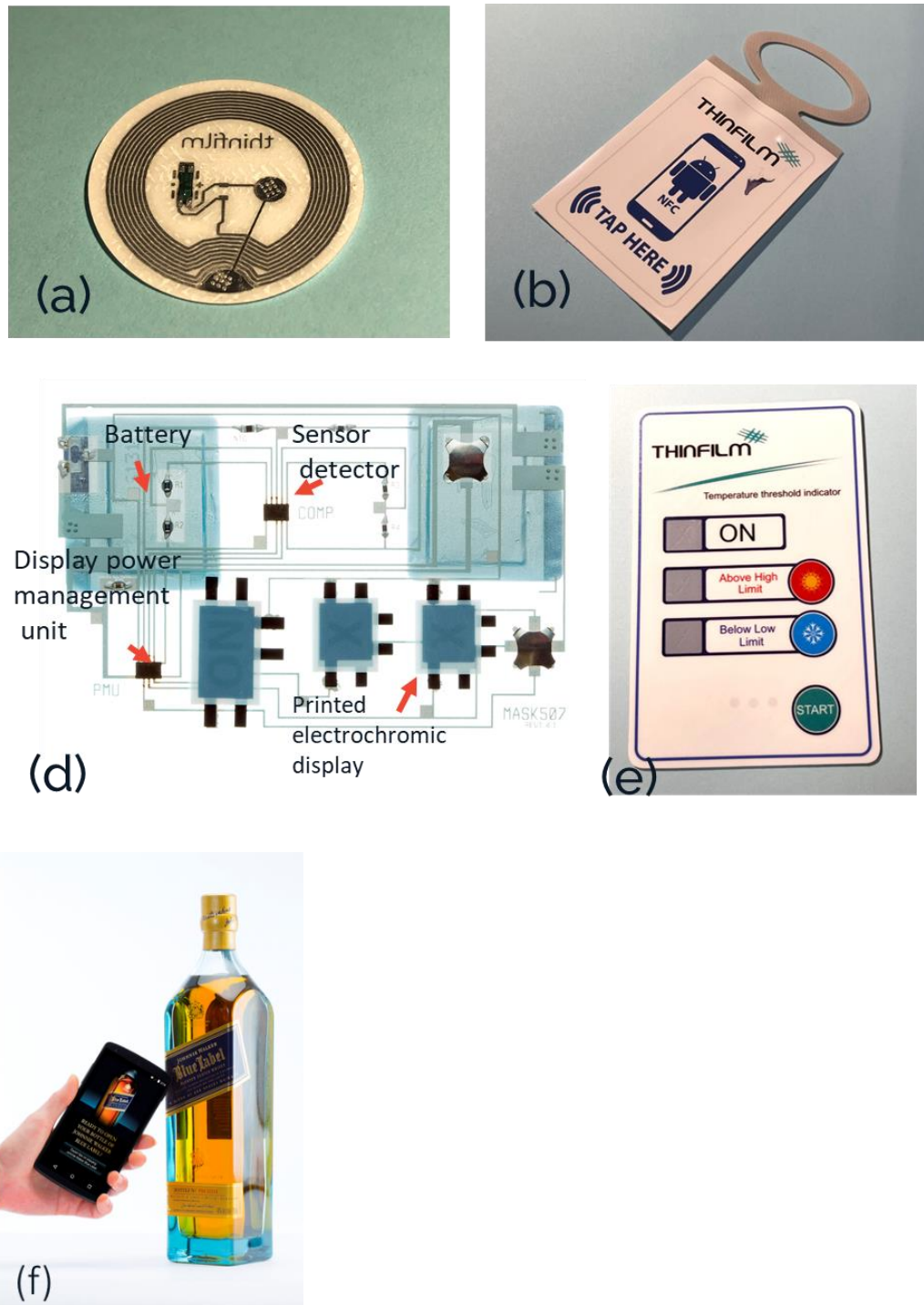


Figure 7.6: Photographs of (a) an assembled SFC tag, (b) NFC tag for promotion, (c) an assembled temperature sensor label, (e) a finished label, and (f) a sensor label for authentication of factory sealed bottles

3.3 Roll-to-roll tools

Figure 7.7 shows the roll-to-roll equipment for the hybrid fabrication of TFTs. Fifteen, toolsets including metrology and test in various stages of installing and building. The use of 320 mm x 200 m roll of stainless steel foil instead of 300-mm² foil would increase productivity from 10s of millions to billions of dies a year.

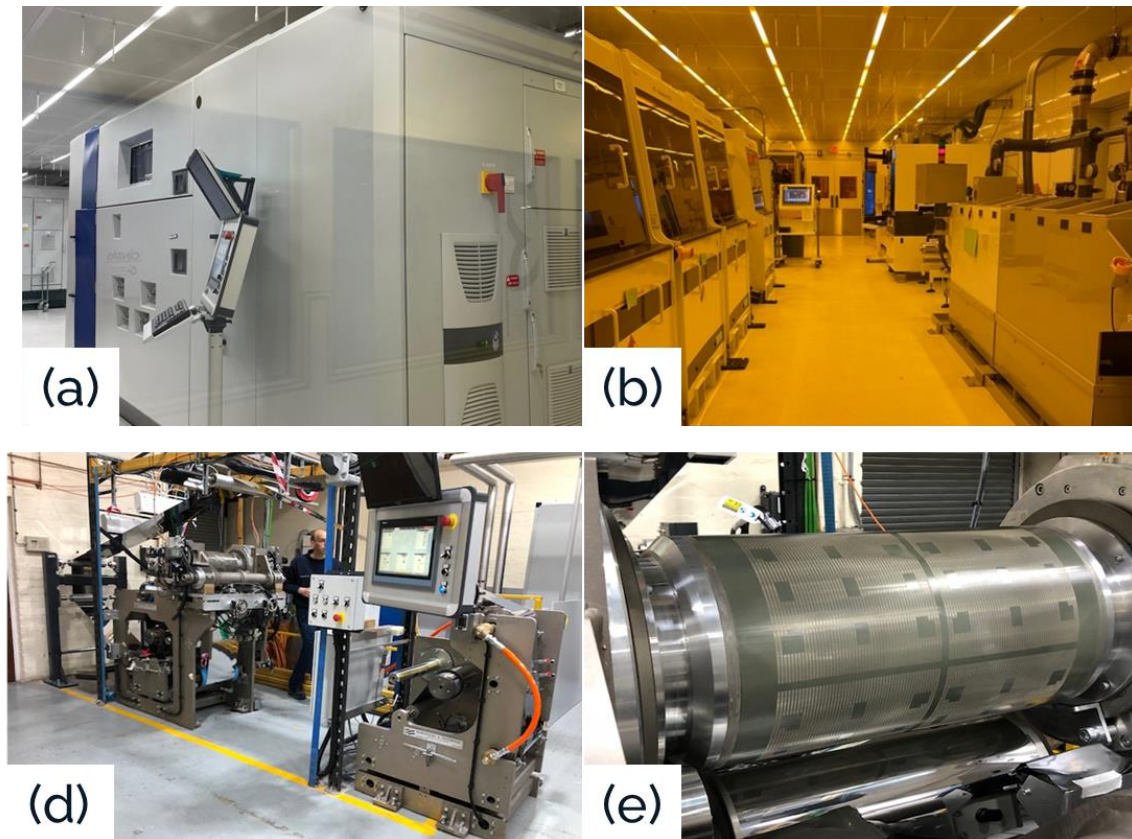


Figure 7.7 Photographs of roll-to-roll equipment: (a) an RIE machine, (b) lithography and etching line, (c) a screen printer, and (d) a rotary screen for N+ ink

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5. Publications

5.1 Journals

First author

1. Ito, M. and Kamath, A. Fabrication and Characterization of Entirely Inkjet-Printed Polysilicon Thin Film Transistors. *Flex. Print. Electron.* 6,015001 (2021)
2. Ito, M. and Kamath, A., Formulation and characterization of screen printable dopant inks, *Flex. Print. Electron.* 6,025004 (2021)
3. Ito, M. and Kamath, A., Slot-die Coating of Silicon Ink for Manufacturing Logic Circuits, *Jpn. J. Appl. Phys.* 60, 101001 (2021)
4. Ito, M. and Kamath, A., Large Area, High Temperature Stainless Steel Foil Substrate for Manufacturing Low-cost and Flexible CMOS Polysilicon TFTs, *J Soc Inf Display.* 1–10 (2022)
5. Ito, M. and Kamath, A., Polysilicon TFTs fabricated using poly-tetrasilane ink., *MRS Commun.* <https://doi.org/10.1557/s43579-022-00152-1> (2022)

Co-author (as Takashima)

6. Chandra, A., Takashima, M., Montague, M., Li, J. and Kamath, A., Screen Printable Semiconductor Grade Inks for N and P type Doping of Polysilicon, *MRS Advances*, 1(14), 965–970 (2016).
7. Chandra, A., Takashima, M. Li, J. Beck, P., Considerations and Methodology to Determine R2R Manufacturing and Scaling of Electronic Devices on Flexible Stainless Steel Foil Substrates, *MRS Advanced* 2, 18,.1029-1036(2017)
8. Chandra, A., Takashima, M. Kamath, A., Silicon and Dopant Ink-Based CMOS TFTs on Flexible Steel Foils, *MRS Advanced* 2, 23,.1259-1256 (2017)

5.2 Conference proceedings

1. Takashima, I. M. *Display Manufacturing Technology Conference* (1998)
2. Takashima, M., Chandra, A. Kamath, A., *Flextech Proceedings* (2015).
3. Takashima, M., Chandra, A. Kamath, A., *SID display week SID Symposium Digest of Technical Papers*, 46, 1 (2015)
4. Trifunovic, M. Chandra, A. Ito, M. Khoo, S. Kamath, A., *International Display Workshops* (2019)

5.3 Invited presentations

1. Flexible Hybrid Electronics for Wearable Applications session at SEMICON West (2015)
2. “International Printing Week” Graphic Communication Department at California Polytechnic State University (2016)
3. The International Symposium on Silent Voice Sensing, the 30th anniversary of JAIST (2020)
4. Material Research Meeting, Yokohama (2021)

5.4 Patents

US patents: Lead inventor

10667397	Electronic device having a plated antenna and/or trace, and methods of making and using the same
10115051	Humidity sensor, wireless device including the same, and methods of making and using the same
9947988	Wireless communication device with integrated ferrite shield and antenna, and methods of manufacturing the same
20190019074	Wireless tags with printed stud sumps, and methods of making and using the same
20180285706	Electronic device having an antenna, metal trace(s) and/or inductor with a printed adhesion promoter thereon, and methods of making and using the same
20190205135	Wireless communication device with integrated ferrite shield and antenna, and methods of manufacturing the same
20170040665	Wireless communication device with integrated ferrite shield and antenna, and methods of manufacturing the same
9359513B1	Dopant inks, methods of making dopant inks, and methods of using dopant inks

US Patents: Co-inventor

8900915	Epitaxial structures and methods of forming the same
8617992	Method of forming metal silicide contact and metal interconnect
8367031	Silane compositions, methods of making the same, method for forming a semiconducting and/or silicon-containing film, and thin film structures formed therefrom
86172992B2	Methods of making metal silicide contacts, interconnects, and/or seed layers
8124040	Methods of making silane compositions
8066805	Metal inks, methods of making the same, and methods for printing and/or forming metal films
7799302	Silane compositions, methods of making the same, method for forming a semiconducting and/or silicon-containing film, and thin film structures formed therefrom
7315068	Interface layer for the fabrication of electronic devices
6957608	Contact print methods
749015	Method of making silane composition
6911385	Interface layer for the fabrication of electronic devices
5962581	Silicone polymer composition, method of forming a pattern and method of forming an insulating film
20190267698	Printed and/or thin film integrated circuit with integrated antenna and methods of making and using the same
20120182636	Printing of contact metal and interconnect metal via seed printing and plating
20110240997	Epitaxial structures, methods of forming the same, and devices including the same
20090020829	Printing of contact metal and interconnect metal via seed printing and plating
20090004370	Metal inks, methods of making the same, and methods for printing and/or forming metal films
20050164480	Interface layer for the fabrication of electronic devices

Japanese Patents

H10-288795	Liquid crystal display, and method of manufacturing the same
H9-179305	Photo patternable material, and method of patterning and coloring the same
H9-172009	Silicone polymer composition, method of forming a pattern and method of forming an insulating film
H9-61615	Color-filter with black matrix, and method of manufacturing the same
H8-262422	Color-filter with black matrix and liquid crystal display, and method of manufacturing the same
H11-077879	Metal oxide conductive thin film, and method of fabrication the same